

	L #	Hits	Search Text	DBs
1	L1	93761	(speculative\$3 sequen\$4 order) near10 (instruction execut\$3)	USPAT; US-PGPUB
2	L2	1692	(indicat\$3 flag tag bit field mode) near10 (allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near20 1	USPAT; US-PGPUB
3	L3	445	((speculative\$3 sequen\$4 order) and (instruction execut\$3)).ab,ti. and 2	USPAT; US-PGPUB
4	L8	95938	(speculative\$3 sequen\$4 order predict\$3) near10 (instruction execut\$3)	USPAT; US-PGPUB
5	L9	1793	(indicat\$3 flag tag bit field mode) near10 (allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near20 8	USPAT; US-PGPUB
6	L10	527	((speculative\$3 sequen\$4 order predict\$3) and (instruction execut\$3)).ab,ti. and 9	USPAT; US-PGPUB
7	L11	31579	(speculative\$3 sequen\$4 order predict\$3) near10 (instruction execut\$3)	EPO; JPO; DERWENT; IBM_TDB
8	L12	157	(indicat\$3 flag tag bit field mode) near10 (allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near20 11	EPO; JPO; DERWENT; IBM_TDB
9	L13	62	9 near10 speculative\$3	USPAT; US-PGPUB
10	L19	95947	(speculat\$6 sequen\$4 order predict\$3) near10 (instruction execut\$3)	USPAT; US-PGPUB
11	L22	31612	(speculat\$6 sequen\$4 order predict\$3) near10 (instruction execut\$3)	EPO; JPO; DERWENT; IBM_TDB
12	L33	1734	(indicat\$3 flag tag bit field mode) near10 ((allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near10 19)	USPAT; US-PGPUB
13	L34	563	((speculat\$6 sequen\$4 order predict\$3 load) and (instruction execut\$3)).ab,ti. and 33	USPAT; US-PGPUB
14	L35	25	(indicat\$3 flag tag bit field mode) near10 ((allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near10 22) not 12	EPO; JPO; DERWENT; IBM_TDB
15	L36	56467	(speculat\$6 order predict\$3) near10 (instruction execut\$3)	USPAT; US-PGPUB
16	L37	273	(indicat\$3 flag tag bit field mode) near10 ((allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near10 36) and 34 not 13	USPAT; US-PGPUB
17	L38	243	34 not (37 13)	USPAT; US-PGPUB

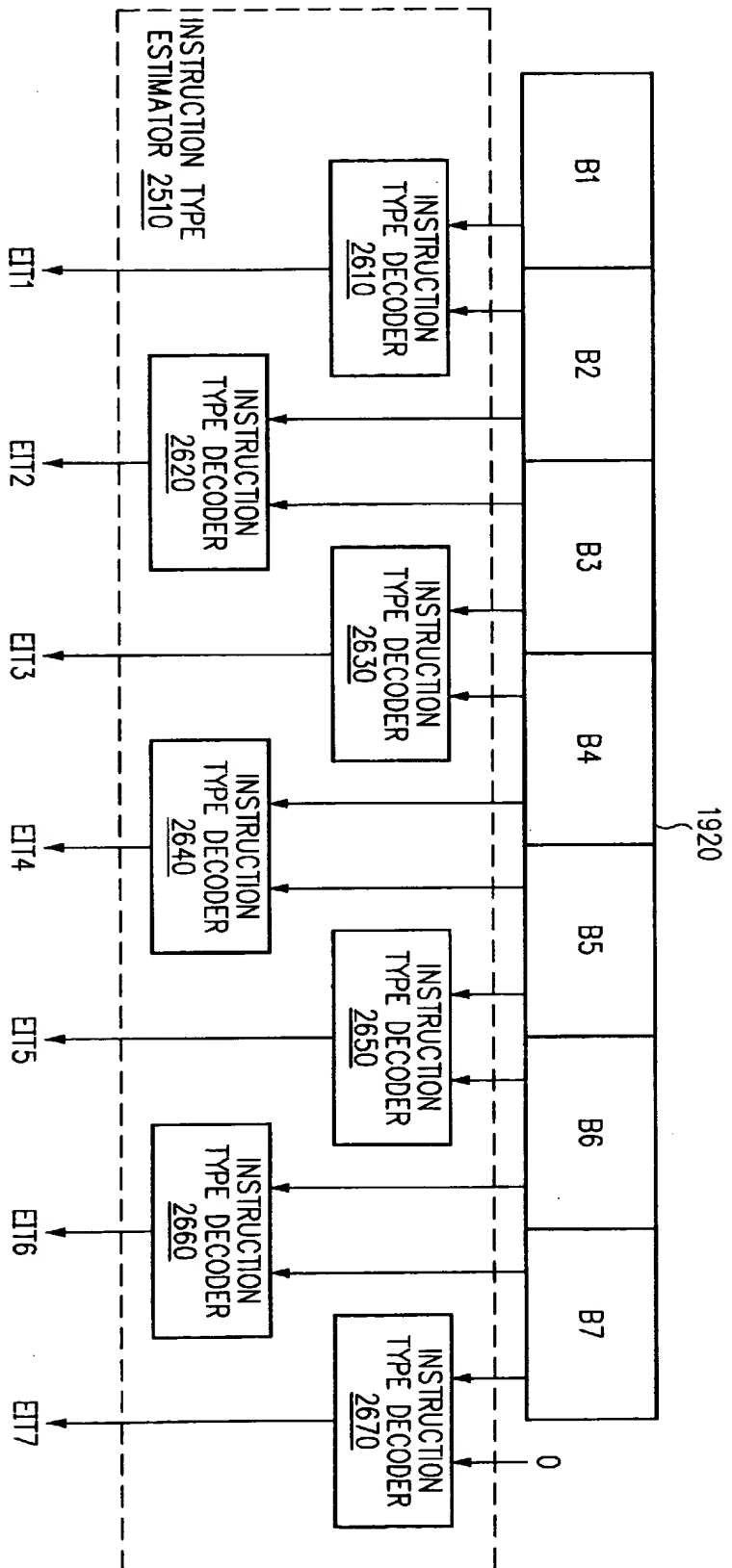


FIG. 26

	Docum ent ID	U	Title	Current OR
1	JP 20032 08335 A	<input type="checkbox"/>	WINDOW MENU TEST SYSTEM	
2	JP 20010 34167 A	<input type="checkbox"/>	ARITHMETIC UNIT AND CRYPTOGRAM PROCESSOR	
3	JP 41134 7892 A	<input type="checkbox"/>	MIXED FLOW PRODUCTION SYSTEM	
4	JP 10154 073 A	<input type="checkbox"/>	DEVICE AND METHOD FOR MANAGING DATA DEPENDENCY	
5	JP 08251 017 A	<input type="checkbox"/>	TEST CONTROL CIRCUIT FOR SEQUENTIAL CIRCUIT, AND TEST METHOD THEREOF	
6	JP 07311 660 A	<input type="checkbox"/>	METHOD FOR PROCESSING DATA IN SOFTWARE CONTROL SYSTEM FOR EARLY DETECTING OBSTACLE	
7	JP 07302 189 A	<input type="checkbox"/>	ADDER AND ADDING METHOD	
8	JP 07078 088 A	<input type="checkbox"/>	DEVICE FOR PROCESSING PLURAL TIMES OF INTERRUPTION AT PROCESSOR SYSTEM, METHOD FOR REACTING TO INTERRUPTIONS FROM PLURAL INTERRUPTION TRIGGERS AT PROCESSOR SYSTEM, METHOD AND DEVICE FOR SIMULTANEOUS T	
9	JP 06242 949 A	<input type="checkbox"/>	QUEUE MANAGEMENT TYPE INSTRUCTION CACHE	
10	JP 04096 496 A	<input type="checkbox"/>	CONTROL DATA TRANSMISSION SYSTEM	
11	JP 02142 272 A	<input type="checkbox"/>	FACSIMILE EQUIPMENT	
12	JP 01036 399 A	<input type="checkbox"/>	VOICE ALARM OUTPUT DEVICE FOR OUTBOARD MOTOR	
13	WO 20040 01586 A1	<input type="checkbox"/>	DEVICE AND METHOD FOR PROCESSING A SEQUENCE OF JUMP INSTRUCTIONS	
14	EP 10963 71 A1	<input type="checkbox"/>	A method and apparatus for prefetching instructions	
15	EP 63780 2 A2	<input type="checkbox"/>	Interrupt vector method and apparatus.	
16	US 20030 08875 9 A	<input type="checkbox"/>	Scratch value identification method in e.g. personal computer, involves setting tags associated with data areas of processor to indicate that data areas hold scratch values	
17	US 20020 13823 6 A	<input type="checkbox"/>	Execution result prediction processor increases priority of priority table based on whether predicted value generated using history table and execution result of instruction being executed currently, are similar	
18	US 20010 02095 2 A	<input type="checkbox"/>	Script producing apparatus for proof image producing system, has script producing section for producing script representative of execution order which is recognized by processor based on execution diagram	
19	EP 10469 83 A	<input type="checkbox"/>	Very long instruction word processor executes sub-instructions in parallel and has an exchange system to exchange sub-instructions prior to execution	
20	US 59999 69 A	<input type="checkbox"/>	Message transfer protocol executing method in interrupt handling system connected to network with hard and soft emulated digital modules	

## U.S. PATENT DOCUMENTS

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5,581,774	12/1996	Yoshitake et al.	712/210
5,584,009	12/1996	Ganbay, Jr. et al.	712/210
5,603,006	2/1997	Satake et al.	712/210
5,625,784	4/1997	Purcell	712/210
5,634,027	5/1997	Saito	712/210
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5,784,553	7/1998	Kolawa et al.	712/210
5,961,638	10/1999	Tran	712/210
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6,008,745	12/1999	Zandi et al.	712/210

	Docum ent ID	U	Title	Current OR
21	GB 22758 05 A	<input type="checkbox"/>	Electronic cash register - has expanded macro key functions set so that only operator having manager level to operate register at predetermined time.	
22	EP 56571 2 B	<input type="checkbox"/>	Network structure for parallel processing computer programs - uses large number of highly efficient virtual processors derived from large memory banks in the core of the network	
23	EP 54724 5 B	<input type="checkbox"/>	Image processing method for industrial visual sensor in robot controller - fetches image data from auxiliary memory using flags sequentially in frame memory when production line stopped, executes image processing program and allows failures to be analysed from monitor display	
24	US 41708 32 A	<input type="checkbox"/>	Interactive teaching machine with video recorded material - has recording of events leading to several possible choices and buttons selecting playback of consequences of each choice	
25	GB 14465 35 A	<input type="checkbox"/>	Semi-automatic wiring machine - has target arrangement indicating each terminal in turn to be wired	

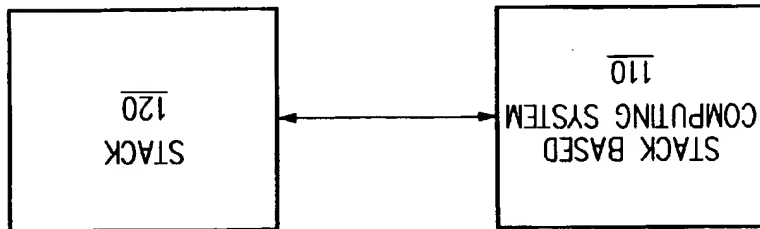


FIG. 1

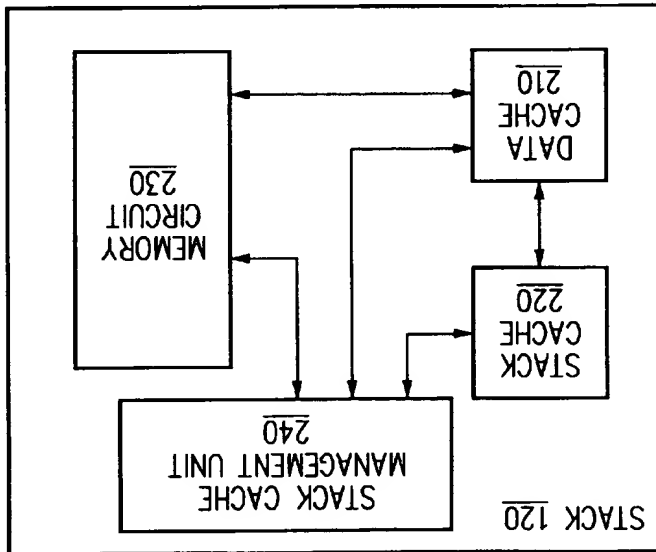


FIG. 2

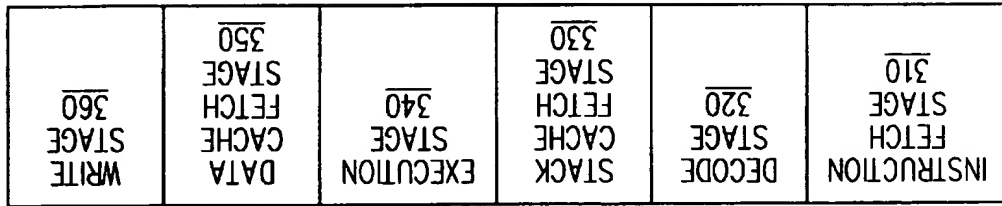


FIG. 3

300

	Docum ent ID	U	Title	Current OR
1	US 20040 05487 2 A1	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/206
2	US 20040 04966 0 A1	<input checked="" type="checkbox"/>	Method and apparatus for clearing hazards using jump instructions	712/219
3	US 20040 00320 5 A1	<input checked="" type="checkbox"/>	Apparatus and method for executing instructions	712/215
4	US 20040 00291 3 A1	<input checked="" type="checkbox"/>	Online trade aggregating system	705/37
5	US 20030 22954 8 A1	<input checked="" type="checkbox"/>	Cash home-delivery system and cash home-delivery method	705/26
6	US 20030 21725 1 A1	<input checked="" type="checkbox"/>	Prediction of load-store dependencies in a processing agent	712/225
7	US 20030 20866 5 A1	<input checked="" type="checkbox"/>	Reducing data speculation penalty with early cache hit/miss prediction	711/169
8	US 20030 20470 5 A1	<input checked="" type="checkbox"/>	Prediction of branch instructions in a data processing apparatus	712/207
9	US 20030 18254 3 A1	<input checked="" type="checkbox"/>	TRAINING LINE PREDICTOR FOR BRANCH TARGETS	712/237
10	US 20030 18228 7 A1	<input checked="" type="checkbox"/>	Interface for an electronic spreadsheet and a database management system	707/10
11	US 20030 18220 3 A1	<input checked="" type="checkbox"/>	Method for supporting shipment of virtual shopping mall	705/26
12	US 20030 18205 0 A1	<input checked="" type="checkbox"/>	Apparatus and method for diagnosis of vehicular system	701/114
13	US 20030 17708 6 A1	<input checked="" type="checkbox"/>	Integrated order pre-matching system	705/37
14	US 20030 16367 0 A1	<input checked="" type="checkbox"/>	Re-encoding illegal OP codes into a single illegal OP code to accommodate the extra bits associated with pre-decoded instructions	712/209
15	US 20030 15901 9 A1	<input checked="" type="checkbox"/>	Prediction of instructions in a data processing apparatus	712/207
16	US 20030 15436 2 A1	<input checked="" type="checkbox"/>	Method and system for safe data dependency collapsing based on control-flow speculation	712/216
17	US 20030 14024 5 A1	<input checked="" type="checkbox"/>	Secure mode for processors supporting MMU and interrupts	713/200

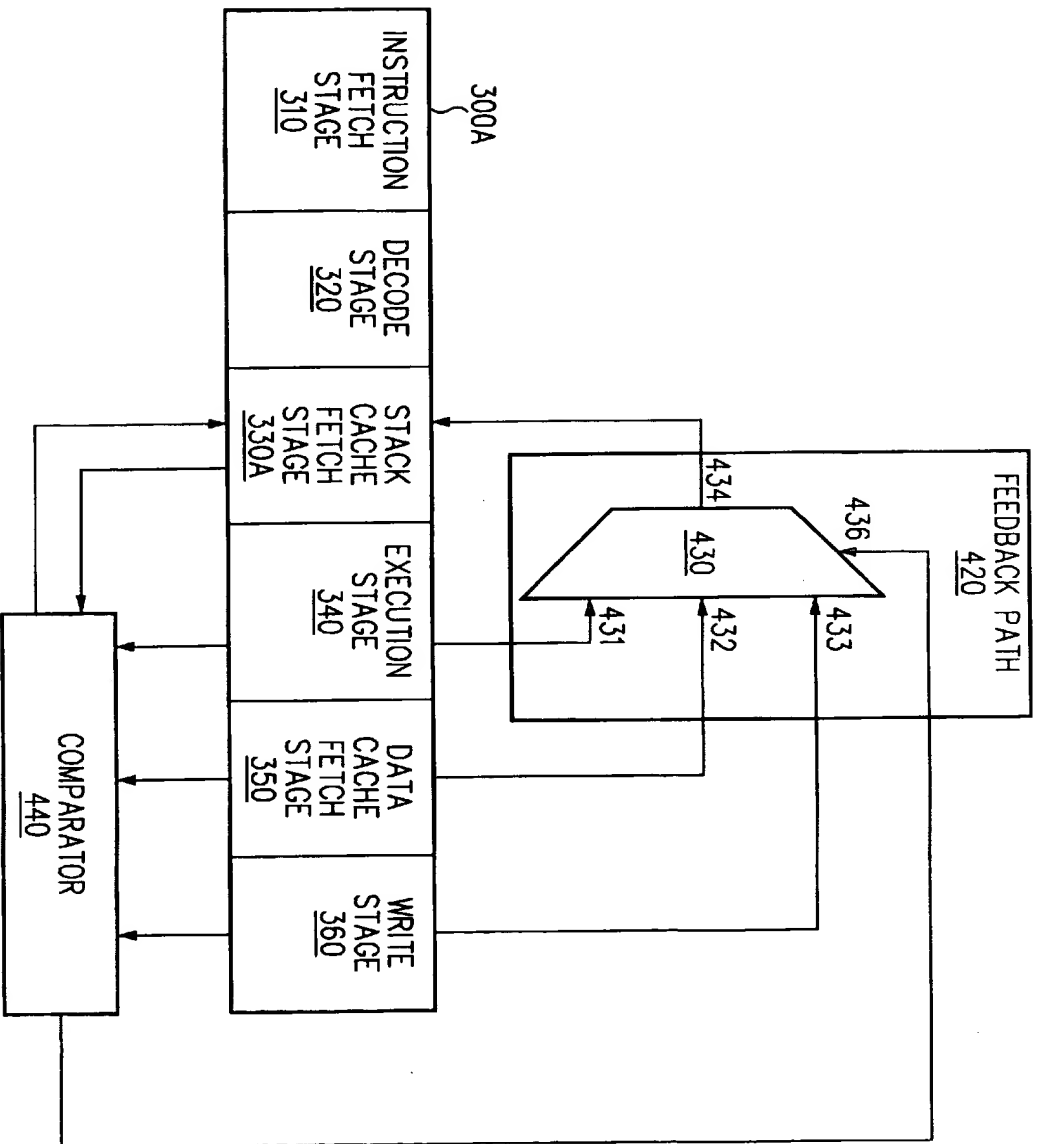


FIG. 4



	Docum ent ID	U	Title	Current OR
18	US 20030 14024 4 A1	<input checked="" type="checkbox"/>	Secure mode for processors supporting MMU	713/200
19	US 20030 14020 5 A1	<input checked="" type="checkbox"/>	Secure mode for processors supporting interrupts	711/163
20	US 20030 13572 2 A1	<input checked="" type="checkbox"/>	Speculative load instructions with retry	712/235
21	US 20030 12606 6 A1	<input checked="" type="checkbox"/>	Electronic communication network ranking for automated market system	705/37
22	US 20030 12606 5 A1	<input checked="" type="checkbox"/>	Order price threshold for automated market system	705/37
23	US 20030 07911 3 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/205
24	US 20030 07006 0 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
25	US 20030 05608 7 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
26	US 20030 05608 6 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/207
27	US 20030 04098 4 A1	<input checked="" type="checkbox"/>	Image processing apparatus, method of placing order for expendables of image processing apparatus, storage medium, and program	705/27
28	US 20030 03880 8 A1	<input checked="" type="checkbox"/>	Method, apparatus and article of manufacture for a sequencer in a transform/lighting module capable of processing multiple independent execution threads	345/506
29	US 20030 02844 6 A1	<input checked="" type="checkbox"/>	Web-enabled method and system for searching correct model data indicative of a product to be purchased online	705/27
30	US 20030 02451 8 A1	<input checked="" type="checkbox"/>	Computer system, particularly for simulation of human perception via sense organs	124/50
31	US 20030 02072 0 A1	<input checked="" type="checkbox"/>	Method, apparatus and article of manufacture for a sequencer in a transform/lighting module capable of processing multiple independent execution threads	345/506
32	US 20020 19445 6 A1	<input checked="" type="checkbox"/>	System and method for register renaming	712/217
33	US 20020 15700 0 A1	<input checked="" type="checkbox"/>	Software hint to improve the branch target prediction accuracy	712/239
34	US 20020 15236 8 A1	<input checked="" type="checkbox"/>	Processor with value predictor	712/226

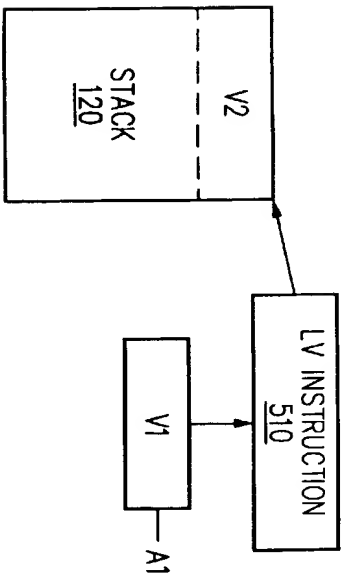


FIG. 5a

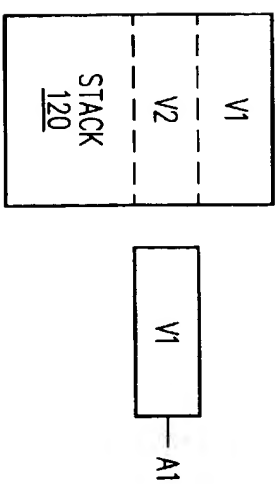


FIG. 5b

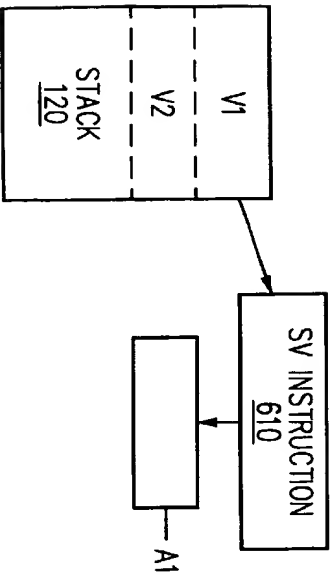


FIG. 6a

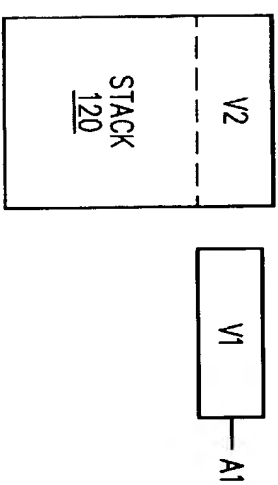
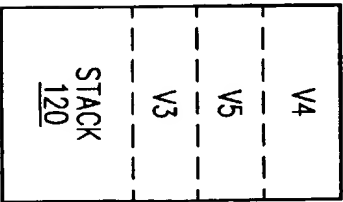
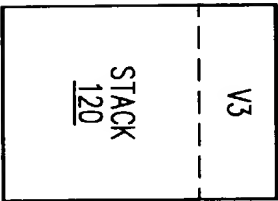
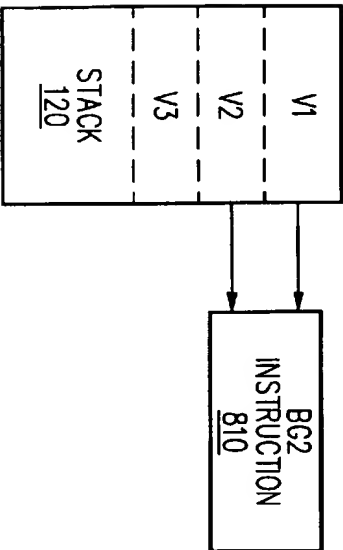
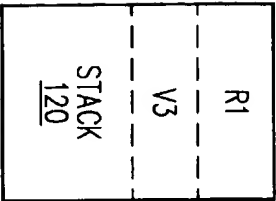
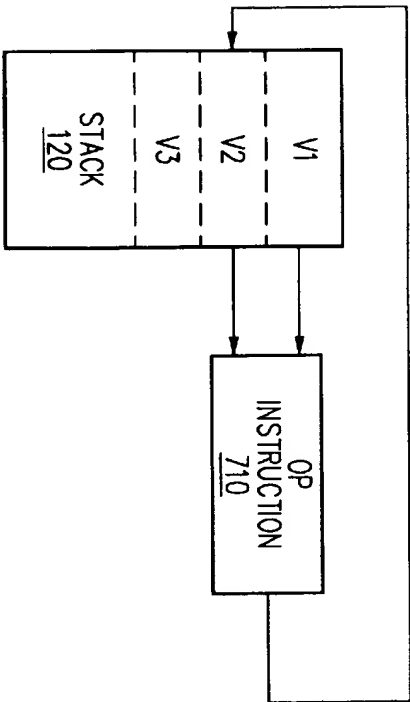


FIG. 6b

	Docum ent ID	U	Title	Current OR
35	US 20020 14409 8 A1	<input checked="" type="checkbox"/>	Register rotation prediction and precomputation	712/221
36	US 20020 13823 6 A1	<input checked="" type="checkbox"/>	Processor having execution result prediction function for instruction	702/186
37	US 20020 10778 1 A1	<input checked="" type="checkbox"/>	Compound order handling in an anonymoustrading system	705/37
38	US 20020 09543 8 A1	<input checked="" type="checkbox"/>	Proposed syntax for a synchronized commands execution	715/500 .1
39	US 20020 09191 3 A1	<input checked="" type="checkbox"/>	Re-order buffer managing method and processor	712/218
40	US 20020 08331 2 A1	<input checked="" type="checkbox"/>	Branch Prediction apparatus and process for restoring replaced branch history for use in future branch predictions for an executing program	712/240
41	US 20020 08330 0 A1	<input checked="" type="checkbox"/>	System and method for register renaming	712/203
42	US 20020 07335 7 A1	<input checked="" type="checkbox"/>	Multiprocessor with pair-wise high reliability mode, and method therefore	714/19
43	US 20020 07301 6 A1	<input checked="" type="checkbox"/>	Order execution processing for automated market system	705/37
44	US 20020 04996 1 A1	<input checked="" type="checkbox"/>	Rule-based personalization framework	717/127
45	US 20020 03284 1 A1	<input checked="" type="checkbox"/>	Cache update method and cache update control system employing non-blocking type cache	711/133
46	US 20020 02932 8 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
47	US 20020 01690 3 A1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
48	US 20010 02095 2 A1	<input checked="" type="checkbox"/>	Script producing apparatus and script producing program storage medium	345/704
49	US 20010 01134 3 A1	<input checked="" type="checkbox"/>	System and method for register renaming	712/217
50	US 20010 00712 5 A1	<input checked="" type="checkbox"/>	Computer system with debug facility	712/226
51	US 20010 00475 5 A1	<input checked="" type="checkbox"/>	MECHANISM FOR FREEING REGISTERS ON PROCESSORS THAT PERFORM DYNAMIC OUT-OF-ORDER EXECUTION OF INSTRUCTIONS USING RENAMING REGISTERS	712/217



	Docum ent ID	U	Title	Current OR
52	US 66979 32 B1	<input checked="" type="checkbox"/>	System and method for early resolution of low confidence branches and safe data cache accesses	712/216
53	US 66977 89 B2	<input checked="" type="checkbox"/>	Computer system, particularly for simulation of human perception via sense organs	706/12
54	US 66786 38 B2	<input checked="" type="checkbox"/>	Processor having execution result prediction function for instruction	702/186
55	US 66752 98 B1	<input checked="" type="checkbox"/>	Execution of instructions using op code lengths longer than standard op code lengths to encode data	713/190
56	US 66752 91 B1	<input checked="" type="checkbox"/>	Hardware device for parallel processing of any instruction within a set of instructions	712/236
57	US 66717 98 B1	<input checked="" type="checkbox"/>	Configurable branch prediction for a processor performing speculative execution	712/234
58	US 66507 31 B1	<input checked="" type="checkbox"/>	Simulator for simulating an intelligent network	379/15. 01
59	US 66503 30 B2	<input checked="" type="checkbox"/>	Graphics system and method for processing multiple independent execution threads	345/506
60	US 66474 90 B2	<input checked="" type="checkbox"/>	Training line predictor for branch targets	712/233
61	US 66474 85 B2	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
62	US 66474 63 B2	<input checked="" type="checkbox"/>	Cache update method and cache update control system employing non-blocking type cache	711/118
63	US 66403 15 B1	<input checked="" type="checkbox"/>	Method and apparatus for enhancing instruction level parallelism	714/17
64	US 66369 59 B1	<input checked="" type="checkbox"/>	Predictor miss decoder updating line predictor storing instruction fetch address and alignment information upon instruction decode termination condition	712/204
65	US 66339 70 B1	<input checked="" type="checkbox"/>	Processor with registers storing committed/speculative data and a RAT state history recovery mechanism with retire pointer	712/217
66	US 66151 88 B1	<input checked="" type="checkbox"/>	Online trade aggregating system	705/37
67	US 65981 54 B1	<input checked="" type="checkbox"/>	Precoding branch instructions to reduce branch-penalty in pipelined processors	712/237
68	US 65739 00 B1	<input checked="" type="checkbox"/>	Method, apparatus and article of manufacture for a sequencer in a transform/lighting module capable of processing multiple independent execution threads	345/537
69	US H0020 64 H	<input checked="" type="checkbox"/>	Automated fixed income trading	705/37
70	US 65570 95 B1	<input checked="" type="checkbox"/>	Scheduling operations using a dependency matrix	712/216
71	US 65464 78 B1	<input checked="" type="checkbox"/>	Line predictor entry with location pointers and control information for corresponding instructions in a cache line	712/204
72	US 65265 02 B1	<input checked="" type="checkbox"/>	Apparatus and method for speculatively updating global branch history with branch prediction prior to resolution of branch outcome	712/239
73	US 65164 05 B1	<input checked="" type="checkbox"/>	Method and system for safe data dependency collapsing based on control-flow speculation	712/216
74	US 65021 88 B1	<input checked="" type="checkbox"/>	Dynamic classification of conditional branches in global history branch prediction	712/234

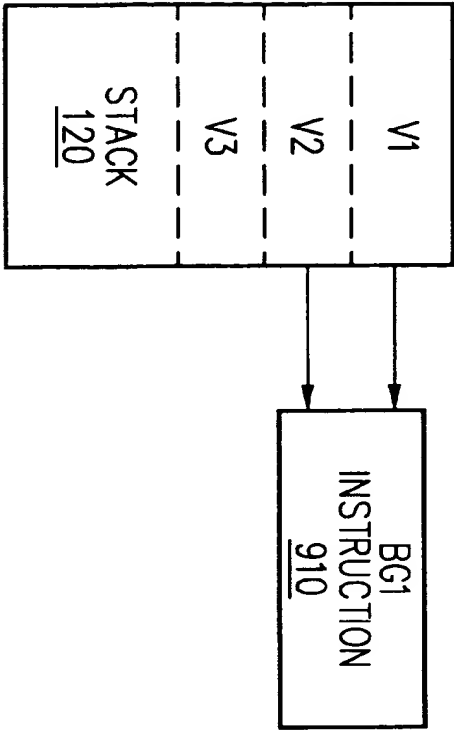


FIG. 9a

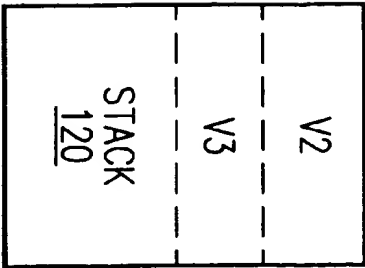


FIG. 9b

	Document ID	U	Title	Current OR
75	US 65021 81 B1	<input checked="" type="checkbox"/>	Method and apparatus for an enhanced processor	712/32
76	US 64842 51 B1	<input checked="" type="checkbox"/>	Updating condition status register based on instruction specific modification information in set/clear pair upon instruction commit in out-of-order processor	712/23
77	US 64386 21 B1	<input checked="" type="checkbox"/>	In-memory modification of computer programs	719/331
78	US 64011 93 B1	<input checked="" type="checkbox"/>	Dynamic data prefetching based on program counter and addressing mode	712/207
79	US 63935 53 B1	<input checked="" type="checkbox"/>	Acknowledgement mechanism for just-in-time delivery of load data	712/217
80	US 63706 32 B1	<input checked="" type="checkbox"/>	Method and apparatus that enforces a regional memory model in hierarchical memory systems	711/205
81	US 63603 18 B1	<input checked="" type="checkbox"/>	Configurable branch prediction for a processor performing speculative execution	712/240
82	US 63381 36 B1	<input checked="" type="checkbox"/>	Pairing of load-ALU-store with conditional branch	712/221
83	US 63201 10 B1	<input checked="" type="checkbox"/>	Music game device with automatic setting, method for controlling the same, and storage medium therefor	84/600
84	US 63178 21 B1	<input checked="" type="checkbox"/>	Virtual single-cycle execution in pipelined processors	712/200
85	US 63145 11 B1	<input checked="" type="checkbox"/>	Mechanism for freeing registers on processors that perform dynamic out-of-order execution of instructions using renaming registers	712/217
86	US 62826 63 B1	<input checked="" type="checkbox"/>	Method and apparatus for performing power management by suppressing the speculative execution of instructions within a pipelined microprocessor	713/320
87	US 62826 39 B1	<input checked="" type="checkbox"/>	Configurable branch prediction for a processor performing speculative execution	712/240
88	US 62826 30 B1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
89	US 62791 07 B1	<input checked="" type="checkbox"/>	Branch selectors associated with byte ranges within an instruction cache for rapidly identifying branch predictions	712/239
90	US 62726 19 B1	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
91	US 62601 31 B1	<input checked="" type="checkbox"/>	Method and apparatus for TLB memory ordering	711/210
92	US 62567 20 B1	<input checked="" type="checkbox"/>	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
93	US 62533 16 B1	<input checked="" type="checkbox"/>	Three state branch history using one bit in a branch prediction mechanism	712/239
94	US 62471 23 B1	<input checked="" type="checkbox"/>	Branch prediction mechanism employing branch selectors to select a branch prediction	712/239
95	US 62470 97 B1	<input checked="" type="checkbox"/>	Aligned instruction cache handling of instruction fetches across multiple predicted branch instructions	711/125
96	US 62370 76 B1	<input checked="" type="checkbox"/>	Method for register renaming by copying a 32 bits instruction directly or indirectly to a 64 bits instruction	712/23
97	US 62302 60 B1	<input checked="" type="checkbox"/>	Circuit arrangement and method of speculative instruction execution utilizing instruction history caching	712/239

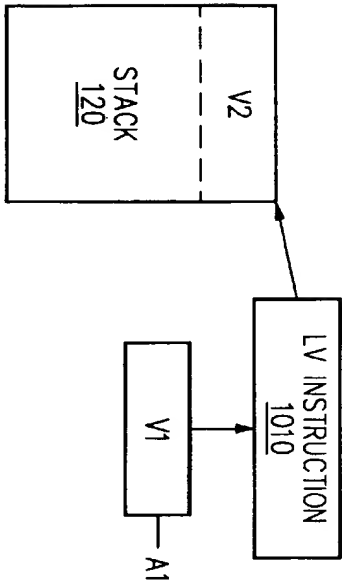


FIG. 10a

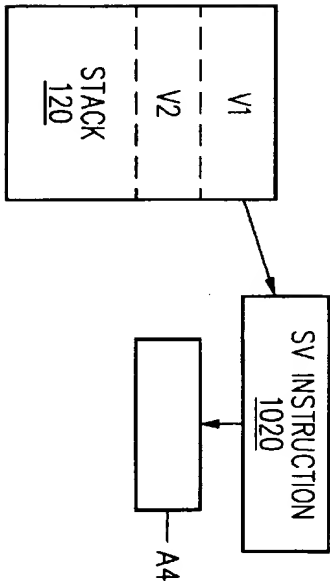


FIG. 10b

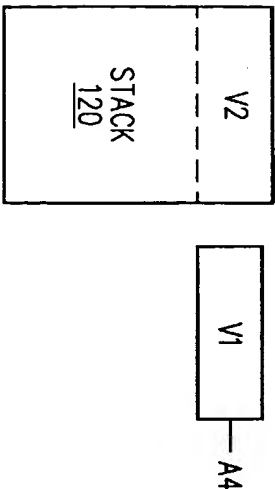


FIG. 10c

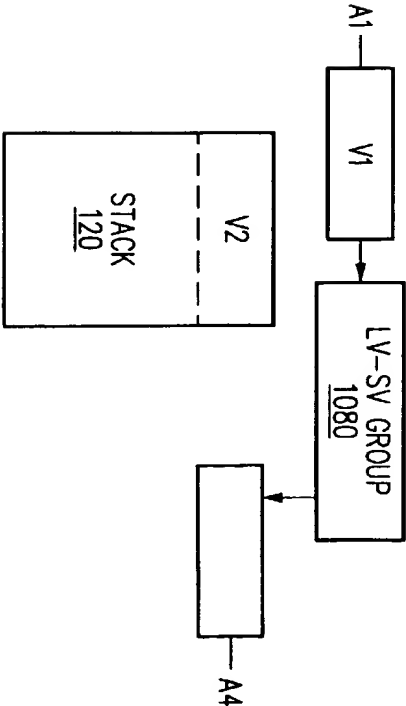


FIG. 10d



	Document ID	U	Title	Current OR
98	US 62166 76 B1	<input checked="" type="checkbox"/>	Internal combustion engine system	123/568 .21
99	US 62161 43 B1	<input checked="" type="checkbox"/>	Apparatus and method for generating animated color coded software traces	715/526
100	US 61890 91 B1	<input checked="" type="checkbox"/>	Apparatus and method for speculatively updating global history and restoring same on branch misprediction detection	712/240
101	US 61784 41 B1	<input checked="" type="checkbox"/>	Method and system in a computer network for the reliable and consistent ordering of client requests	709/203
102	US 61784 38 B1	<input checked="" type="checkbox"/>	Service management system for an advanced intelligent network	709/200
103	US 61482 92 A	<input checked="" type="checkbox"/>	Method for statistics mode reloading and for statistical acquisition according to statistics classes in the storing of a dataset	705/30
104	US 61417 48 A	<input checked="" type="checkbox"/>	Branch selectors associated with byte ranges within an instruction cache for rapidly identifying branch predictions	712/239
105	US 61375 88 A	<input checked="" type="checkbox"/>	Digital reproduction control method and apparatus having autonomous and command control modes	358/1.1 5
106	US 61287 23 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
107	US 61192 22 A	<input checked="" type="checkbox"/>	Combined branch prediction and cache prefetch in a microprocessor	712/238
108	US 61087 77 A	<input checked="" type="checkbox"/>	Configurable branch prediction for a processor performing speculative execution	712/240
109	US 61087 74 A	<input checked="" type="checkbox"/>	Branch prediction with added selector bits to increase branch prediction capacity and flexibility with minimal added bits	712/240
110	US 61015 94 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/41
111	US 60921 81 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/206
112	US 60618 23 A	<input checked="" type="checkbox"/>	Error correcting/decoding apparatus and error correcting/decoding method	714/758
113	US 60556 26 A	<input checked="" type="checkbox"/>	Method and circuit for delayed branch control and method and circuit for conditional-flag rewriting control	712/216
114	US 60556 24 A	<input checked="" type="checkbox"/>	Millicode flags with specialized update and branch instructions	712/208
115	US 60473 69 A	<input checked="" type="checkbox"/>	Flag renaming and flag masks within register alias table	712/217
116	US 60386 54 A	<input checked="" type="checkbox"/>	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
117	US 60386 53 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
118	US 60386 31 A	<input checked="" type="checkbox"/>	Data processing system and method using virtual storage system	710/260
119	US 60292 40 A	<input checked="" type="checkbox"/>	Method for processing instructions for parallel execution including storing instruction sequences along with compounding information in cache	712/23
120	US 60291 46 A	<input checked="" type="checkbox"/>	Method and apparatus for trading securities electronically	705/35

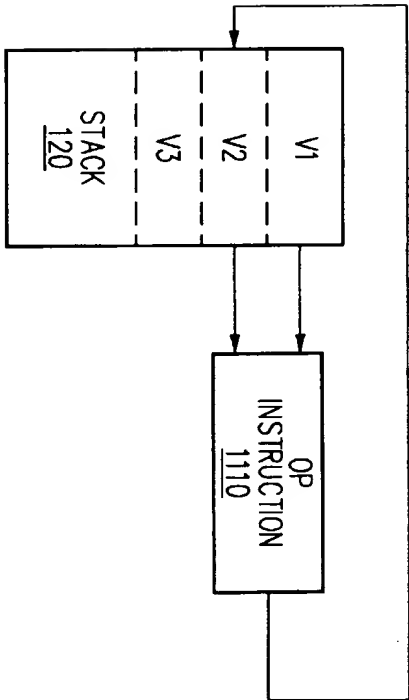


FIG. 11a

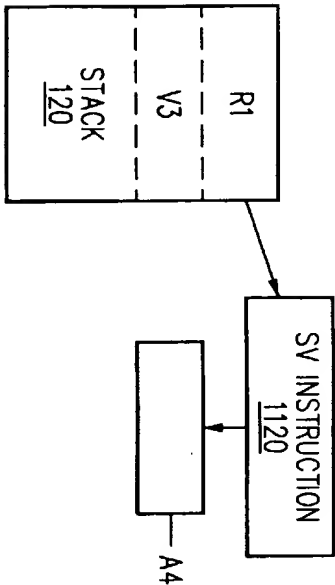


FIG. 11b

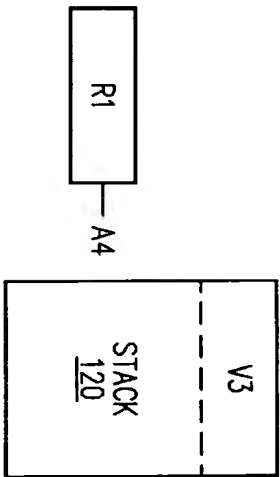


FIG. 11c

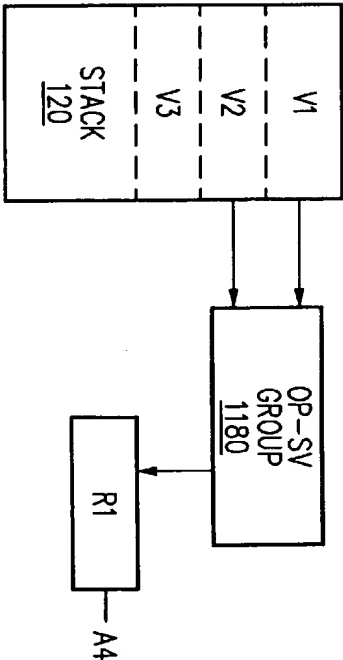


FIG. 11d

	Document ID	U	Title	Current OR
121	US 60214 89 A	<input checked="" type="checkbox"/>	Apparatus and method for sharing a branch prediction unit in a microprocessor implementing a two instruction set architecture	712/239
122	US 60031 28 A	<input checked="" type="checkbox"/>	Number of pipeline stages and loop length related counter differential based end-loop prediction	712/241
123	US 60028 50 A	<input checked="" type="checkbox"/>	Operation sequence user adaptive system and method	719/315
124	US 59960 71 A	<input checked="" type="checkbox"/>	Detecting self-modifying code in a pipelined processor with branch processing by comparing latched store address to subsequent target address	712/238
125	US 59960 69 A	<input checked="" type="checkbox"/>	Method and circuit for delayed branch control and method and circuit for conditional-flag rewriting control	712/234
126	US 59957 49 A	<input checked="" type="checkbox"/>	Branch prediction mechanism employing branch selectors to select a branch prediction	712/239
127	US 59876 03 A	<input checked="" type="checkbox"/>	Apparatus and method for reversing bits using a shifter	712/300
128	US 59789 06 A	<input checked="" type="checkbox"/>	Branch selectors associated with byte ranges within an instruction cache for rapidly identifying branch predictions	712/239
129	US 59745 42 A	<input checked="" type="checkbox"/>	Branch prediction unit which approximates a larger number of branch predictions using a smaller number of branch predictions and an alternate target indication	712/239
130	US 59745 35 A	<input checked="" type="checkbox"/>	Method and system in data processing system of permitting concurrent processing of instructions of a particular type	712/215
131	US 59665 44 A	<input checked="" type="checkbox"/>	Data speculatable processor having reply architecture	712/32
132	US 59616 38 A	<input checked="" type="checkbox"/>	Branch prediction mechanism employing branch selectors to select a branch prediction	712/239
133	US 59616 29 A	<input checked="" type="checkbox"/>	High performance, superscalar-based computer system with out-of-order instruction execution	712/23
134	US 59564 95 A	<input checked="" type="checkbox"/>	Method and system for processing branch instructions during emulation in a data processing system	703/26
135	US 59548 16 A	<input checked="" type="checkbox"/>	Branch selector prediction	712/239
136	US 59535 20 A	<input checked="" type="checkbox"/>	Address translation buffer for data processing system emulation mode	703/26
137	US 59516 78 A	<input checked="" type="checkbox"/>	Method and apparatus for controlling conditional branch execution in a data processor	712/237
138	US 59338 60 A	<input checked="" type="checkbox"/>	Multiprobe instruction cache with instruction-based probe hint generation and training whereby the cache bank or way to be accessed next is predicted	711/213
139	US 59305 21 A	<input checked="" type="checkbox"/>	Reorder buffer architecture for accessing partial word operands	712/23
140	US 59238 62 A	<input checked="" type="checkbox"/>	Processor that decodes a multi-cycle instruction into single-cycle micro-instructions and schedules execution of the micro-instructions	712/208
141	US 59207 10 A	<input checked="" type="checkbox"/>	Apparatus and method for modifying status bits in a reorder buffer with a large speculative state	712/216
142	US 59180 30 A	<input checked="" type="checkbox"/>	Device for executing a program of instructions	712/206
143	US 59037 50 A	<input checked="" type="checkbox"/>	Dynamic branch prediction for branch instructions with multiple targets	712/236

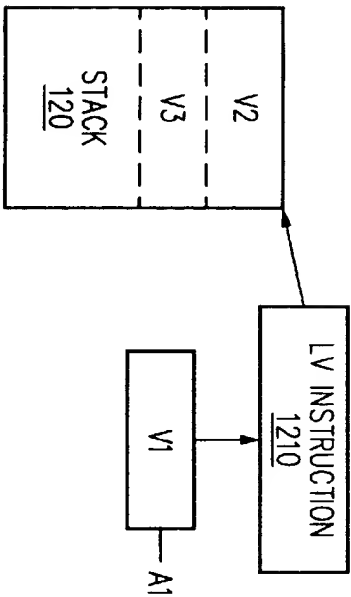


FIG. 12a

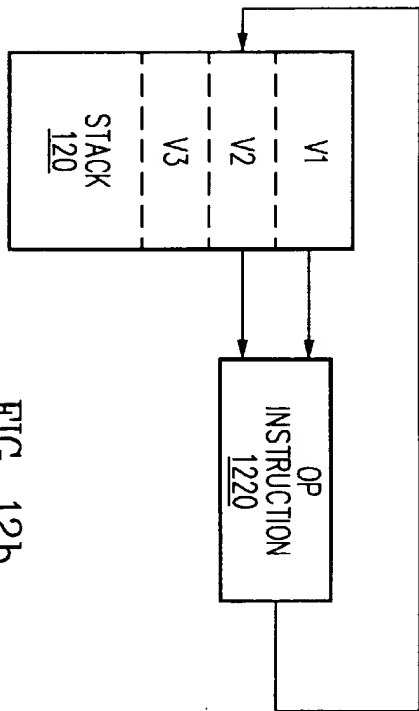


FIG. 12b

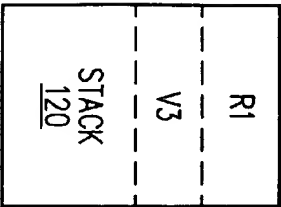


FIG. 12c

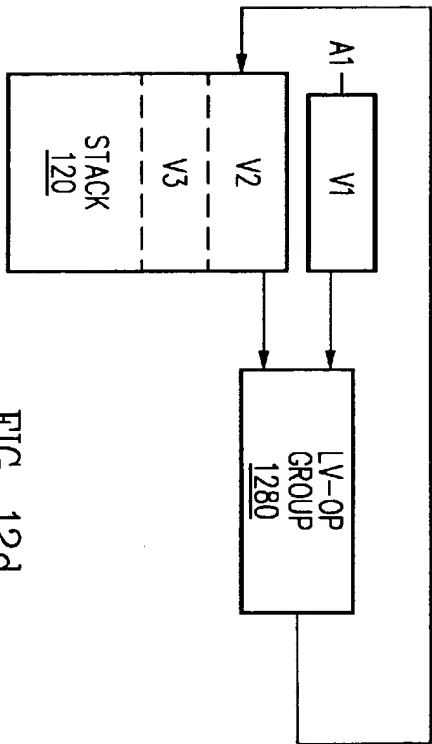


FIG. 12d

	Docum ent ID	U	Title	Current OR
144	US 58992 03 A	<input checked="" type="checkbox"/>	Interactive respiratory regulator	128/204 .23
145	US 58931 65 A	<input checked="" type="checkbox"/>	System and method for parallel execution of memory transactions using multiple memory models, including SSO, TSO, PSO and RMO	711/158
146	US 58929 63 A	<input checked="" type="checkbox"/>	System and method for assigning tags to instructions to control instruction execution	712/23
147	US 58840 61 A	<input checked="" type="checkbox"/>	Apparatus to perform source operand dependency analysis perform register renaming and provide rapid pipeline recovery for a microprocessor capable of issuing and executing multiple instructions out-of-order in a single processor cycle	712/217
148	US 58753 26 A	<input checked="" type="checkbox"/>	Data processing system and method for completing out-of-order instructions	712/244
149	US 58729 65 A	<input checked="" type="checkbox"/>	System and method for performing multiway branches using a visual instruction set	712/236
150	US 58705 79 A	<input checked="" type="checkbox"/>	Reorder buffer including a circuit for selecting a designated mask corresponding to an instruction that results in an exception	712/217
151	US 58705 75 A	<input checked="" type="checkbox"/>	Indirect unconditional branches in data processing system emulation mode	712/209
152	US 58671 63 A	<input checked="" type="checkbox"/>	Graphical user interface for defining and invoking user-customized tool shelf execution sequence	345/840
153	US 58505 21 A	<input checked="" type="checkbox"/>	Apparatus and method for interprocessor communication	709/208
154	US 58482 69 A	<input checked="" type="checkbox"/>	Branch predicting mechanism for enhancing accuracy in branch prediction by reference to data	712/239
155	US 58322 92 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
156	US 58288 60 A	<input checked="" type="checkbox"/>	Data processing device equipped with cache memory and a storage unit for storing data between a main storage or CPU cache memory	712/207
157	US 58227 78 A	<input checked="" type="checkbox"/>	Microprocessor and method of using a segment override prefix instruction field to expand the register file	711/208
158	US 58190 80 A	<input checked="" type="checkbox"/>	Microprocessor using an instruction field to specify condition flags for use with branch instructions and a computer system employing the microprocessor	712/239
159	US 58156 99 A	<input checked="" type="checkbox"/>	Configurable branch prediction for a processor performing speculative execution	712/239
160	US 58092 94 A	<input checked="" type="checkbox"/>	Parallel processing unit which processes branch instructions without decreased performance when a branch is taken	712/233
161	US 58058 78 A	<input checked="" type="checkbox"/>	Method and apparatus for generating branch predictions for multiple branch instructions indexed by a single instruction pointer	712/239
162	US 58024 12 A	<input checked="" type="checkbox"/>	Miniature pan/tilt tracking mount	396/427
163	US 57992 89 A	<input checked="" type="checkbox"/>	Order management system and method considering budget limit	705/400
164	US 57940 31 A	<input checked="" type="checkbox"/>	Distributed processing system for system booting and shutdown in distributed processing environment	713/2
165	US 57940 28 A	<input checked="" type="checkbox"/>	Shared branch prediction structure	712/240

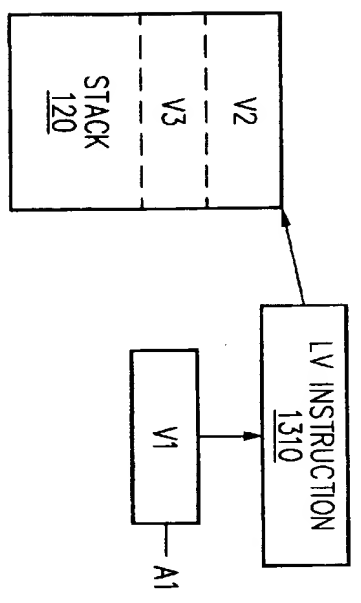


FIG. 13a

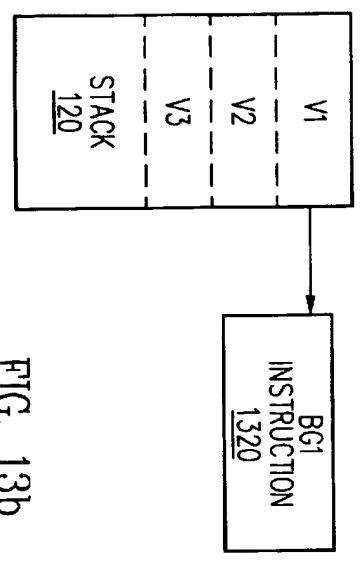


FIG. 13b

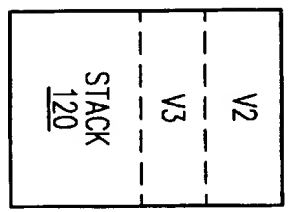


FIG. 13c

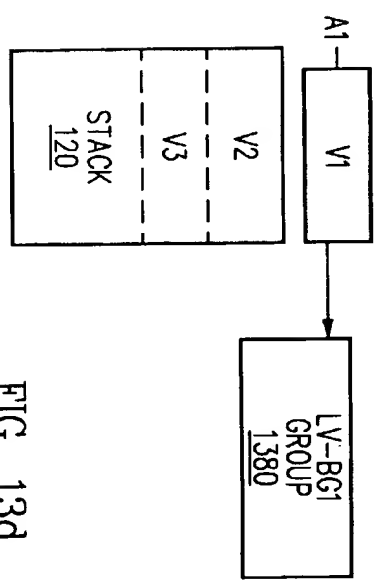


FIG. 13d

	Document ID	U	Title	Current OR
166	US 57846 04 A	<input checked="" type="checkbox"/>	Method and system for reduced run-time delay during conditional branch execution in pipelined processor systems utilizing selectively delayed sequential instruction purging	712/238
167	US 57846 03 A	<input checked="" type="checkbox"/>	Fast handling of branch delay slots on mispredicted branches	712/234
168	US 57747 12 A	<input checked="" type="checkbox"/>	Instruction dispatch unit and method for mapping a sending order of operations to a receiving order	712/245
169	US 57746 85 A	<input checked="" type="checkbox"/>	Method and apparatus for biasing cache LRU for prefetched instructions/data based upon evaluation of speculative conditions	712/205
170	US 57685 74 A	<input checked="" type="checkbox"/>	Microprocessor using an instruction field to expand the condition flags and a computer system employing the microprocessor	712/226
171	US 57652 21 A	<input checked="" type="checkbox"/>	Method and system of addressing which minimize memory utilized to store logical addresses by storing high order bits within a register	711/220
172	US 57614 90 A	<input checked="" type="checkbox"/>	Changing the meaning of a pre-decode bit in a cache memory depending on branch prediction mode	712/239
173	US 57614 74 A	<input checked="" type="checkbox"/>	Operand dependency tracking system and method for a processor that executes instructions out of order	712/217
174	US 57614 69 A	<input checked="" type="checkbox"/>	Method and apparatus for optimizing signed and unsigned load processing in a pipelined processor	712/210
175	US 57375 76 A	<input checked="" type="checkbox"/>	Method and system for efficient instruction execution in a data processing system having multiple prefetch units	711/169
176	US 57352 02 A	<input checked="" type="checkbox"/>	Print sorting method for image forming apparatus with sorter and control system for executing such print sorting method	101/2
177	US 57349 04 A	<input checked="" type="checkbox"/>	Method and system for calling one of a set of routines designed for direct invocation by programs of a second type when invoked by a program of the first type	719/331
178	US 57322 54 A	<input checked="" type="checkbox"/>	Pipeline system branch history table storing branch instruction addresses and target addresses with inhibit bits	712/240
179	US 57301 45 A	<input checked="" type="checkbox"/>	Interactive respiratory regulator	600/595
180	US 57014 48 A	<input checked="" type="checkbox"/>	Detecting segment limit violations for branch target when the branch unit does not supply the linear address	712/233
181	US 56995 06 A	<input checked="" type="checkbox"/>	Method and apparatus for fault testing a pipelined processor	714/37
182	US 56921 68 A	<input checked="" type="checkbox"/>	Prefetch buffer using flow control bit to identify changes of flow within the code stream	712/237
183	US 56897 20 A	<input checked="" type="checkbox"/>	High-performance superscalar-based computer system with out-of-order instruction execution	712/23
184	US 56805 78 A	<input checked="" type="checkbox"/>	Microprocessor using an instruction field to specify expanded functionality and a computer system employing same	711/154
185	US 56665 06 A	<input checked="" type="checkbox"/>	Apparatus to dynamically control the out-of-order execution of load/store instructions in a processor capable of dispatching, issuing and executing multiple instructions in a single processor cycle	712/216
186	US 56550 96 A	<input checked="" type="checkbox"/>	Method and apparatus for dynamic scheduling of instructions to ensure sequentially coherent data in a processor employing out-of-order execution	712/200
187	US 56528 58 A	<input checked="" type="checkbox"/>	Method for prefetching pointer-type data structure and information processing apparatus therefor	711/137

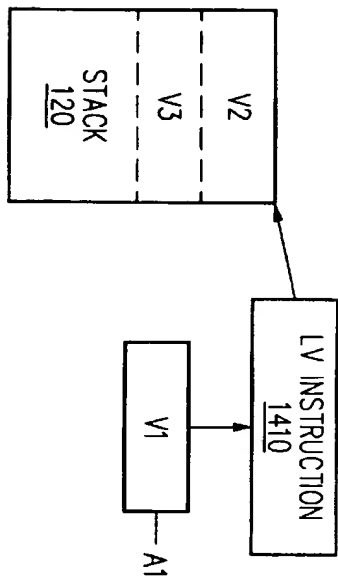


FIG. 14a

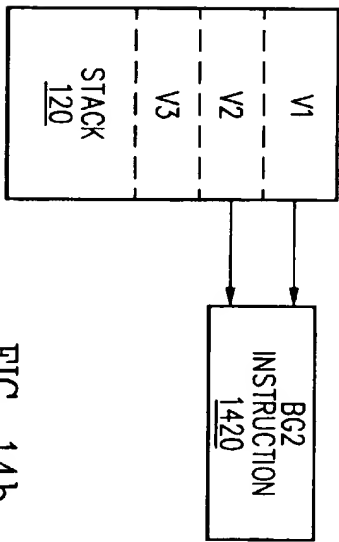


FIG. 14b

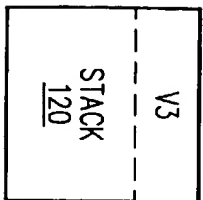


FIG. 14c

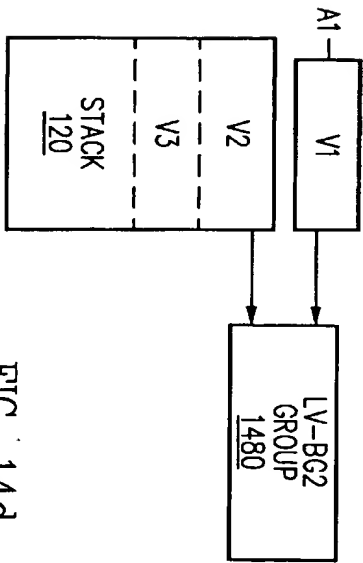


FIG. 14d



	Docum ent ID	U	Title	Current OR
188	US 56503 41 A	<input checked="" type="checkbox"/>	Process for fabricating CMOS Device	438/217
189	US 56447 59 A	<input checked="" type="checkbox"/>	Apparatus and method for processing a jump instruction preceded by a skip instruction	712/240
190	US 56279 84 A	<input checked="" type="checkbox"/>	Apparatus and method for entry allocation for a buffer resource utilizing an internal two cycle pipeline	712/200
191	US 56258 35 A	<input checked="" type="checkbox"/>	Method and apparatus for reordering memory operations in a superscalar or very long instruction word processor	712/23
192	US 56257 89 A	<input checked="" type="checkbox"/>	Apparatus for source operand dependency analyses register renaming and rapid pipeline recovery in a microprocessor that issues and executes multiple instructions out-of-order in a single cycle	712/217
193	US 56153 50 A	<input checked="" type="checkbox"/>	Apparatus to dynamically control the out-of-order execution of load-store instructions in a processor capable of dispatching, issuing and executing multiple instructions in a single processor cycle	712/218
194	US 56088 86 A	<input checked="" type="checkbox"/>	Block-based branch prediction using a target finder array storing target sub-addresses	712/239
195	US 56049 12 A	<input checked="" type="checkbox"/>	System and method for assigning tags to instructions to control instruction execution	712/23
196	US 55985 46 A	<input checked="" type="checkbox"/>	Dual-architecture super-scalar pipeline	712/209
197	US 55926 84 A	<input checked="" type="checkbox"/>	Store queue including a byte order tracking mechanism for maintaining data coherency	710/52
198	US 55926 34 A	<input checked="" type="checkbox"/>	Zero-cycle multi-state branch cache prediction data processing system and method thereof	712/239
199	US 55772 59 A	<input checked="" type="checkbox"/>	Instruction processor control system using separate hardware and microcode control signals to control the pipelined execution of multiple classes of machine instructions	712/41
200	US 55600 32 A	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23

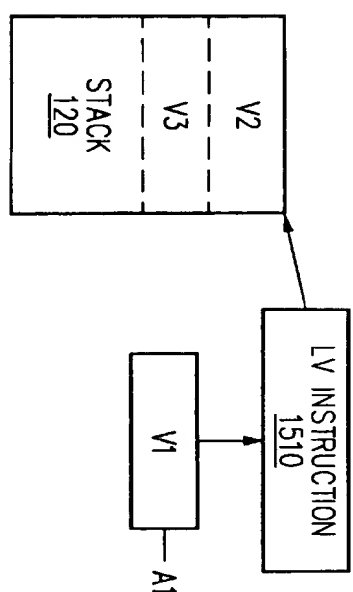


FIG. 15a

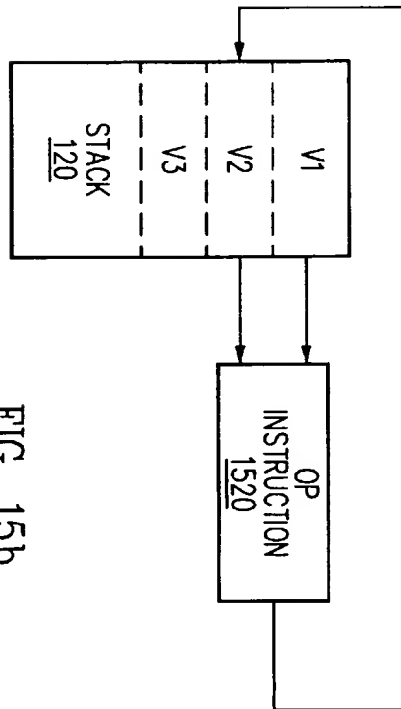


FIG. 15b

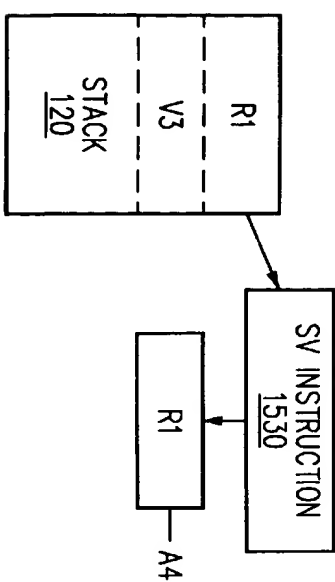


FIG. 15c

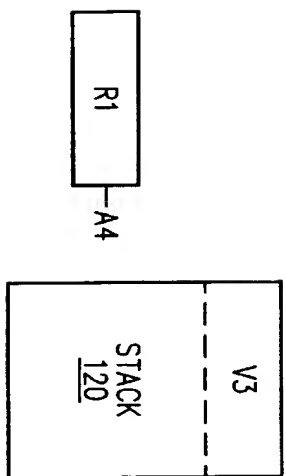


FIG. 15d

	Docum ent ID	U	Title	Current OR
1	US 20040 03083 8 A1	<input type="checkbox"/>	Instruction cache way prediction for jump targets	711/137
2	US 20040 02499 9 A1	<input checked="" type="checkbox"/>	Micro-sequence execution in a processor	712/245
3	US 20040 00695 7 A1	<input checked="" type="checkbox"/>	PROGRAMMABLE FUNCTION CONTROL FOR COMBINE	56/10.2 G
4	US 20040 00672 8 A1	<input checked="" type="checkbox"/>	Method and device for simultaneous testing of a plurality of integrated circuits	714/724
5	US 20030 23355 9 A1	<input checked="" type="checkbox"/>	Data processing apparatus and data processing method	713/189
6	US 20030 21024 6 A1	<input checked="" type="checkbox"/>	Network management card for use in a system for screen image capturing	345/520
7	US 20030 18790 5 A1	<input checked="" type="checkbox"/>	Scheduling tasks quickly in a sequential order	718/100
8	US 20030 14401 2 A1	<input checked="" type="checkbox"/>	Information providing apparatus, computer program product and information providing method	455/456 .1
9	US 20030 14025 3 A1	<input checked="" type="checkbox"/>	Method of and apparatus for detecting creation of set user identification (setuid) files, and computer program for enabling such detection	713/201
10	US 20030 12079 0 A1	<input checked="" type="checkbox"/>	Processor with multiple-pass non-sequential packet classification feature	709/230
11	US 20030 11949 7 A1	<input checked="" type="checkbox"/>	Test system for remotely testing switches within a telecommunications network	455/424
12	US 20030 10997 5 A1	<input checked="" type="checkbox"/>	Agricultural vehicle	701/50
13	US 20030 09373 6 A1	<input checked="" type="checkbox"/>	System and method enabling hierarchical execution of a test executive subsequence	714/738
14	US 20030 07910 9 A1	<input checked="" type="checkbox"/>	Methods and apparatus for dynamic very long instruction word sub-instruction selection for execution time parallelism in an indirect very long instruction word processor	712/24
15	US 20030 07005 1 A1	<input checked="" type="checkbox"/>	Methods and apparatus for utilizing flash burst mode to improve processor performance	711/167
16	US 20030 02624 9 A1	<input checked="" type="checkbox"/>	Inter-nodal data transfer system and data transfer apparatus	370/360
17	US 20030 02384 7 A1	<input checked="" type="checkbox"/>	DATA PROCESSING SYSTEM, RECORDING DEVICE, DATA PROCESSING METHOD AND PROGRAM PROVIDING MEDIUM	713/169

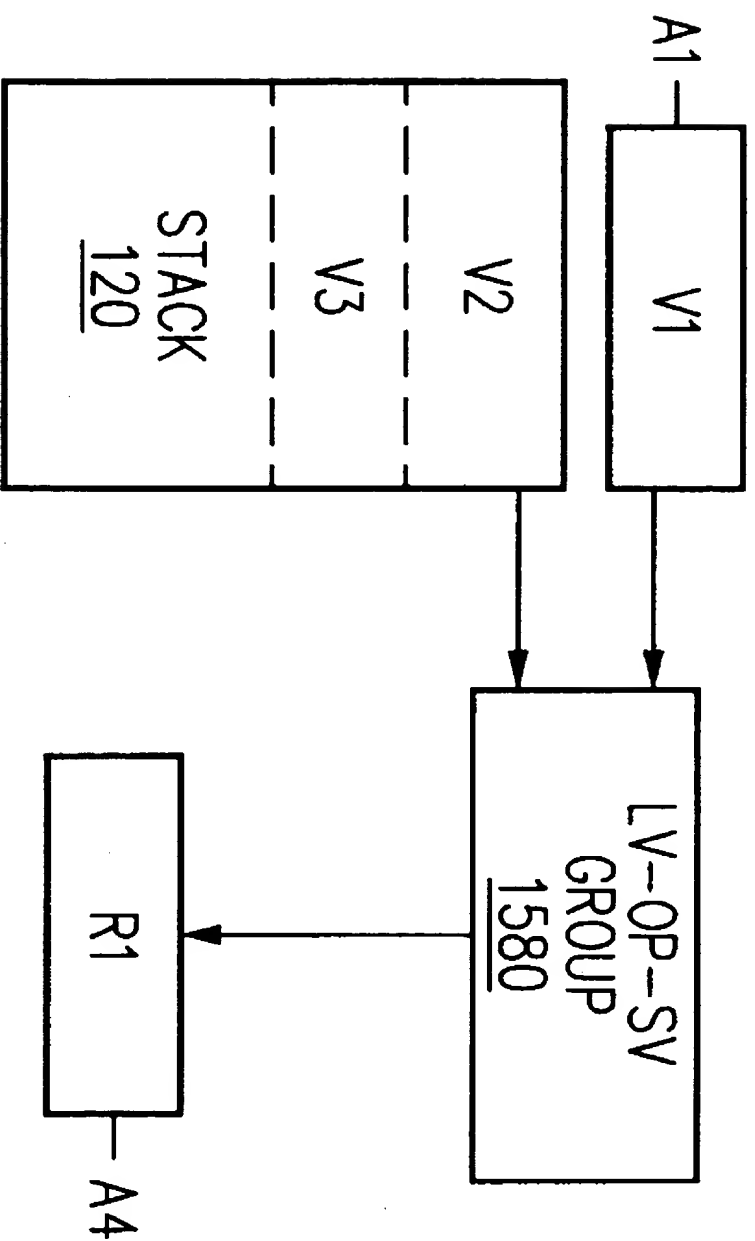
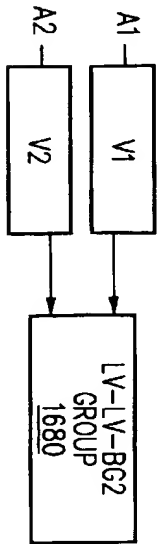
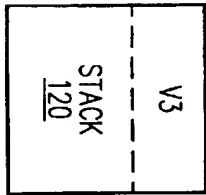
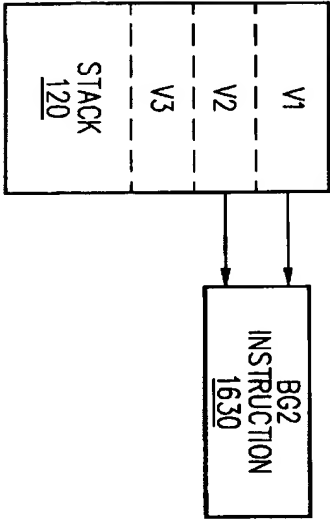
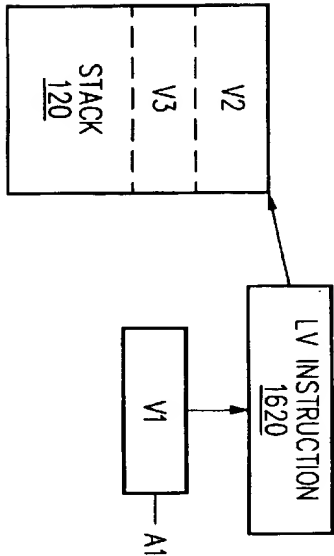
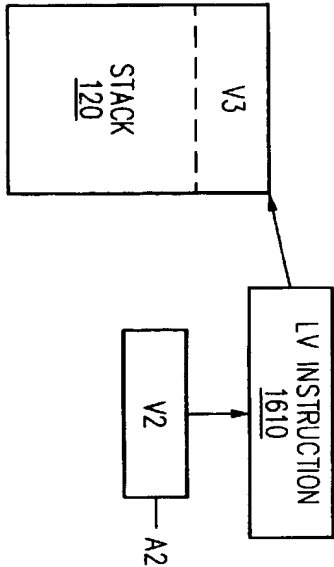


FIG. 15e

	Docum ent ID	U	Title	Current OR
18	US 20030 00931 3 A1	<input checked="" type="checkbox"/>	Real-time alert mechanism for monitoring and controlling field assets via wireless and internet technologies	702/188
19	US 20030 00253 7 A1	<input checked="" type="checkbox"/>	Method and apparatus for controlling the timing of a communication device	370/503
20	US 20020 15704 2 A1	<input checked="" type="checkbox"/>	Algorithmically programmable memory tester with breakpoint trigger, error jamming and 'scope mode that memorizes target sequences	714/45
21	US 20020 11157 0 A1	<input checked="" type="checkbox"/>	MICROCONTROLLER BASED MASSAGE SYSTEM	601/15
22	US 20020 10803 0 A1	<input checked="" type="checkbox"/>	Method and system for performing permutations using permutation instructions based on modified omega and flip stages	712/300
23	US 20020 07832 0 A1	<input checked="" type="checkbox"/>	Methods and apparatus for instruction addressing in indirect VLIW processors	712/24
24	US 20020 03122 0 A1	<input checked="" type="checkbox"/>	Method and system for performing permutations using permutation instructions based on butterfly networks	380/37
25	US 20020 02865 9 A1	<input checked="" type="checkbox"/>	Test system for remotely testing switches within a telecommunications network	455/67. 11
26	US 20010 02917 9 A1	<input checked="" type="checkbox"/>	Test system for remotely testing switches within a telecommunications network	455/423
27	US 66815 51 B1	<input checked="" type="checkbox"/>	Programmable function control for combine	56/10.2 G
28	US 66788 15 B1	<input checked="" type="checkbox"/>	Apparatus and method for reducing power consumption due to cache and TLB accesses in a processor front-end	711/205
29	US 66657 92 B1	<input checked="" type="checkbox"/>	Interface to a memory system for a processor having a replay system	712/219
30	US 66648 33 B1	<input checked="" type="checkbox"/>	Dual-edge function clock generator and method of deriving clocking signals for executing reduced instruction sequences in a re-programmable I/O interface	327/170
31	US 66548 78 B1	<input checked="" type="checkbox"/>	Register bit scanning	712/234
32	US 65811 52 B2	<input checked="" type="checkbox"/>	Methods and apparatus for instruction addressing in indirect VLIW processors	712/24
33	US 65781 33 B1	<input checked="" type="checkbox"/>	MIMD array of single bit processors for processing logic equations in strict sequential order	712/21
34	US 65670 84 B1	<input checked="" type="checkbox"/>	Lighting effect computation circuit and method therefore	345/426
35	US 65562 08 B1	<input checked="" type="checkbox"/>	Network management card for use in a system for screen image capturing	345/520
36	US 65427 38 B2	<input checked="" type="checkbox"/>	Test system for remotely testing switches within a telecommunications network	455/424
37	US 65421 99 B1	<input checked="" type="checkbox"/>	Cadence editing	348/459



	Docum ent ID	U	Title	Current OR
38	US 65389 98 B1	<input checked="" type="checkbox"/>	Rolling out high bandwidth connection services in geographical areas covering several central offices	370/241
39	US 65360 34 B1	<input checked="" type="checkbox"/>	Method for modifying code sequences and related device	717/110
40	US 65079 21 B1	<input checked="" type="checkbox"/>	Trace fifo management	714/45
41	US 64697 04 B1	<input checked="" type="checkbox"/>	System and method for combined execution of graphics primitive data sets	345/553
42	US 64670 36 B1	<input checked="" type="checkbox"/>	Methods and apparatus for dynamic very long instruction word sub-instruction selection for execution time parallelism in an indirect very long instruction word processor	712/24
43	US 64571 52 B1	<input checked="" type="checkbox"/>	Device and method for testing a device through resolution of data into atomic operations	714/738
44	US 64534 12 B1	<input checked="" type="checkbox"/>	Method and apparatus for reissuing paired MMX instructions singly during exception handling	712/244
45	US 64183 36 B1	<input checked="" type="checkbox"/>	MR tomography apparatus and method for suppressing stimulation of an examination subject	600/410
46	US 63701 46 B1	<input checked="" type="checkbox"/>	Method and apparatus for non-disruptive addition of a new node to an inter-nodal network	370/400
47	US 63628 25 B1	<input checked="" type="checkbox"/>	Real-time combination of adjacent identical primitive data sets in a graphics call sequence	345/522
48	US 63569 94 B1	<input checked="" type="checkbox"/>	Methods and apparatus for instruction addressing in indirect VLIW processors	712/24
49	US 62759 82 B1	<input checked="" type="checkbox"/>	Method and device enabling a fixed program to be developed	717/168
50	US 62759 20 B1	<input checked="" type="checkbox"/>	Mesh connected computed	712/14
51	US 62533 06 B1	<input checked="" type="checkbox"/>	Prefetch instruction mechanism for processor	712/207
52	US 62532 87 B1	<input checked="" type="checkbox"/>	Using three-dimensional storage to make variable-length instructions appear uniform in two dimensions	711/125
53	US 62438 48 B1	<input checked="" type="checkbox"/>	Process for analyzing complex structures and system for implementing a process of this type	716/1
54	US 62405 08 B1	<input checked="" type="checkbox"/>	Decode and execution synchronized pipeline processing using decode generated memory read queue with stop entry to allow execution generated memory read	712/219
55	US 62302 78 B1	<input checked="" type="checkbox"/>	Microprocessor with functional units that can be selectively coupled	713/324
56	US 62300 06 B1	<input checked="" type="checkbox"/>	Test system for remotely testing switches within a telecommunications network	455/424
57	US 62126 28 B1	<input checked="" type="checkbox"/>	Mesh connected computer	712/226
58	US 61733 89 B1	<input checked="" type="checkbox"/>	Methods and apparatus for dynamic very long instruction word sub-instruction selection for execution time parallelism in an indirect very long instruction word processor	712/24
59	US 61700 38 B1	<input checked="" type="checkbox"/>	Trace based instruction caching	711/125
60	US 61673 30 A	<input checked="" type="checkbox"/>	Dynamic power management of systems	700/295

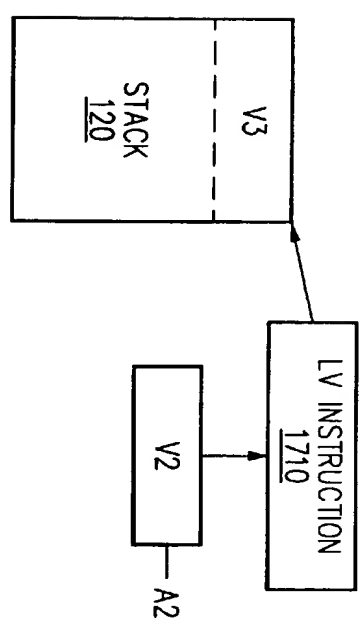


FIG. 17a

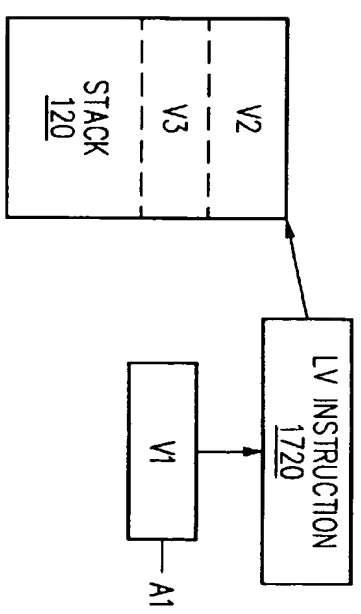


FIG. 17b

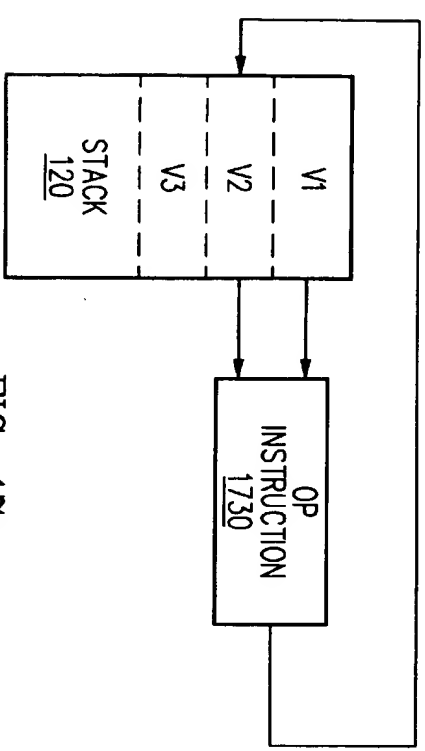


FIG. 17c

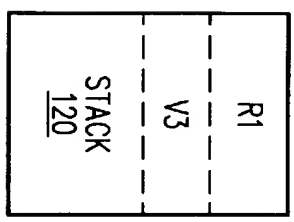


FIG. 17d



	Docum ent ID	U	Title	Current OR
61	US 61579 64 A	<input checked="" type="checkbox"/>	Method for specifying concurrent execution of a string of I/O command blocks in a chain structure	710/5
62	US 61517 05 A	<input checked="" type="checkbox"/>	Efficient use of the base register auto-increment feature of memory access instructions	717/153
63	US 61443 21 A	<input checked="" type="checkbox"/>	Microprocessor dedicated to processing of bit streams in a system of compression/decompression of animated images	341/67
64	US 61339 38 A	<input checked="" type="checkbox"/>	Descriptor mechanism for assuring indivisible execution of AV/C operations	725/80
65	US 61338 59 A	<input checked="" type="checkbox"/>	Microprocessor dedicated to processing of bit streams in a system of compression/decompression of animated images	341/67
66	US 61231 74 A	<input checked="" type="checkbox"/>	Apparatus and method for automatically performing fluid changes	184/1.5
67	US 61223 20 A	<input checked="" type="checkbox"/>	Circuit for motion estimation in digitized video sequence encoders	375/240
68	US 60919 30 A	<input checked="" type="checkbox"/>	Customizable interactive textbook	434/362
69	US 60853 14 A	<input checked="" type="checkbox"/>	Central processing unit including APX and DSP cores and including selectable APX and DSP execution modes	712/213
70	US 60790 08 A	<input checked="" type="checkbox"/>	Multiple thread multiple data predictive coded parallel processing system and method	712/11
71	US 60761 44 A	<input checked="" type="checkbox"/>	Method and apparatus for identifying potential entry points into trace segments	711/125
72	US 60650 40 A	<input checked="" type="checkbox"/>	Computer system having agent retracting method and agent returning method	709/202
73	US 60397 02 A	<input checked="" type="checkbox"/>	Microcontroller based massage system	601/15
74	US 60322 47 A	<input checked="" type="checkbox"/>	Central processing unit including APX and DSP cores which receives and processes APX and DSP instructions	712/35
75	US 60187 86 A	<input checked="" type="checkbox"/>	Trace based instruction caching	711/4
76	US 60165 44 A	<input checked="" type="checkbox"/>	Apparatus and method for tracking changes in address size and for different size retranslate second instruction with an indicator from address size	712/234
77	US 60119 08 A	<input checked="" type="checkbox"/>	Gated store buffer for an advanced microprocessor	714/19
78	US 59833 24 A	<input checked="" type="checkbox"/>	Data prefetch control method for main storage cache for protecting prefetched data from replacement before utilization thereof	711/137
79	US 59628 39 A	<input checked="" type="checkbox"/>	Apparatus programmable to perform a user defined sequence of actions	235/472 .01
80	US 59580 45 A	<input checked="" type="checkbox"/>	Start of access instruction configured to indicate an access mode for fetching memory operands in a microprocessor	712/229
81	US 59419 80 A	<input checked="" type="checkbox"/>	Apparatus and method for parallel decoding of variable-length instructions in a superscalar pipelined data processing system	712/204
82	US 59338 50 A	<input checked="" type="checkbox"/>	Instruction unit having a partitioned cache	711/125
83	US 59266 44 A	<input checked="" type="checkbox"/>	Instruction formats/instruction encoding	712/22

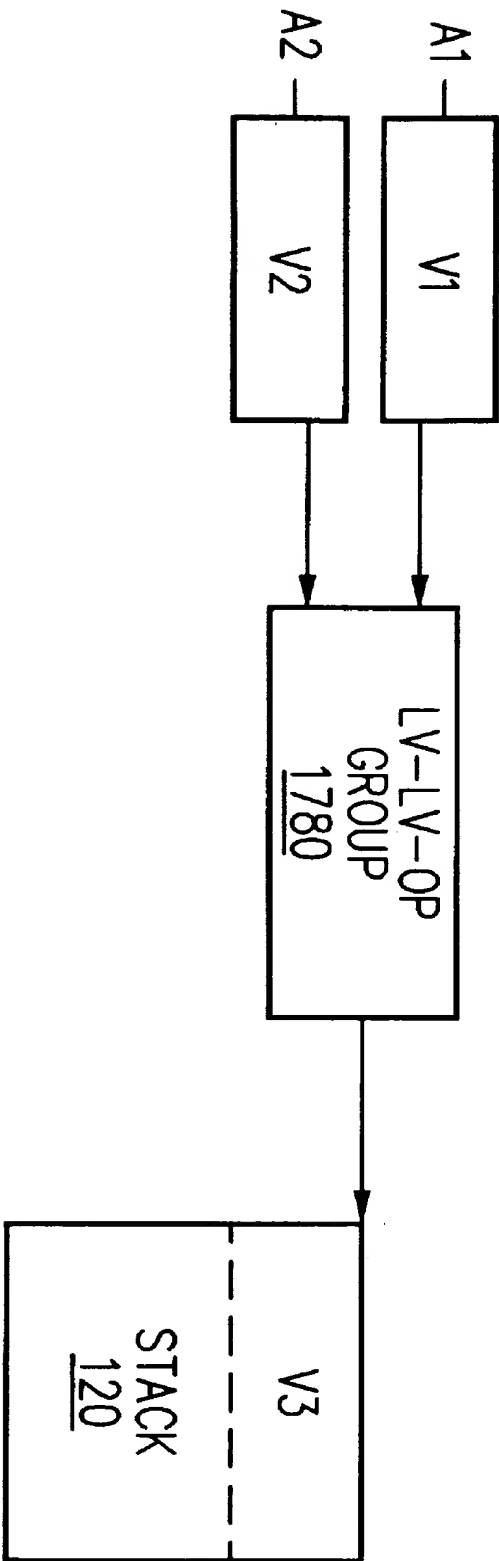


FIG. 17e

	Docum ent ID	U	Title	Current OR
84	US 59238 96 A	<input checked="" type="checkbox"/>	Method for sequencing execution of I/O command blocks in a chain structure by setting hold-off flags and configuring a counter in each I/O command block	710/5
85	US 59220 65 A	<input checked="" type="checkbox"/>	Processor utilizing a template field for encoding instruction sequences in a wide-word format	712/24
86	US 59058 83 A	<input checked="" type="checkbox"/>	Verification system for circuit simulator	703/17
87	US 58981 20 A	<input checked="" type="checkbox"/>	Auto-play apparatus for arpeggio tones	84/638
88	US 58929 69 A	<input checked="" type="checkbox"/>	Method for concurrently executing a configured string of concurrent I/O command blocks within a chain to perform a raid 5 I/O operation	710/5
89	US 58929 06 A	<input checked="" type="checkbox"/>	Apparatus and method for preventing theft of computer devices	713/202
90	US 58812 63 A	<input checked="" type="checkbox"/>	Non-instruction base register addressing in a data processing apparatus	712/217
91	US 58812 59 A	<input checked="" type="checkbox"/>	Input operand size and hi/low word selection control in data processing systems	712/210
92	US 58570 88 A	<input checked="" type="checkbox"/>	System for configuring memory space for storing single decoder table, reconfiguring same space for storing plurality of decoder tables, and selecting one configuration based on encoding scheme	712/210
93	US 58527 29 A	<input checked="" type="checkbox"/>	Code segment replacement apparatus and real time signal processor using same	712/225
94	US 58505 67 A	<input checked="" type="checkbox"/>	Method for specifying concurrent execution of a string of I/O command blocks in a chain structure	710/5
95	US 58480 26 A	<input checked="" type="checkbox"/>	Integrated circuit with flag register for block selection of nonvolatile cells for bulk operations	365/238 .5
96	US 58369 89 A	<input checked="" type="checkbox"/>	Method and apparatus for controlling an implanted medical device in a time-dependent manner	607/27
97	US 58093 20 A	<input checked="" type="checkbox"/>	High-performance multi-processor having floating point unit	712/34
98	US 58023 38 A	<input checked="" type="checkbox"/>	Method of self-parallelizing and self-parallelizing multiprocessor using the method	712/217
99	US 57970 34 A	<input checked="" type="checkbox"/>	Method for specifying execution of only one of a pair of I/O command blocks in a chain structure	710/24
100	US 57940 63 A	<input checked="" type="checkbox"/>	Instruction decoder including emulation using indirect specifiers	712/23
101	US 57937 61 A	<input checked="" type="checkbox"/>	Communication switching system having a user facility system and a base switching system	370/377
102	US 57686 21 A	<input checked="" type="checkbox"/>	Chain manager for use in executing a chain of I/O command blocks	710/24
103	US 57614 77 A	<input checked="" type="checkbox"/>	Methods for safe and efficient implementations of virtual machines	718/1
104	US 57581 87 A	<input checked="" type="checkbox"/>	Method for enhancing performance of a RAID 1 read operation using a pair of I/O command blocks in a chain structure	710/24
105	US 57428 22 A	<input checked="" type="checkbox"/>	Multithreaded processor which dynamically discriminates a parallel execution and a sequential execution of threads	718/102

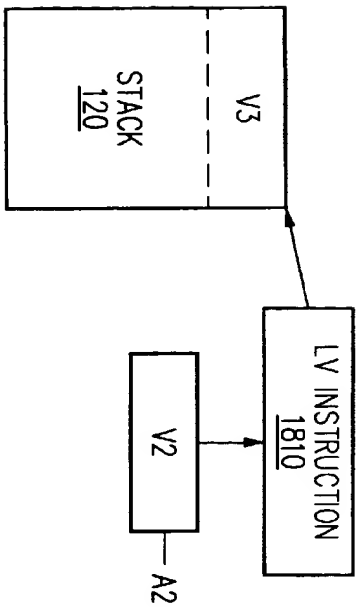


FIG. 18a

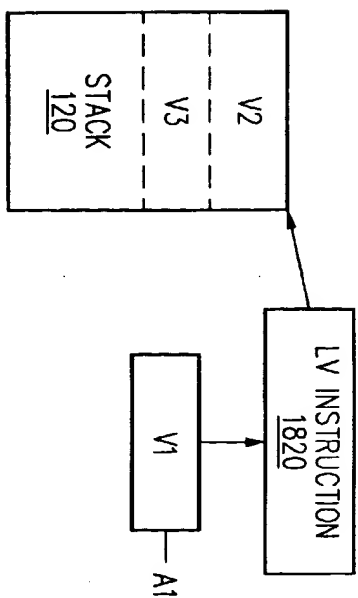


FIG. 18b

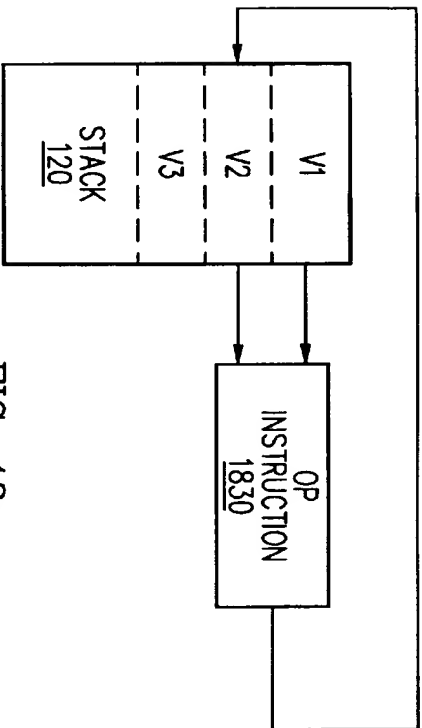


FIG. 18c

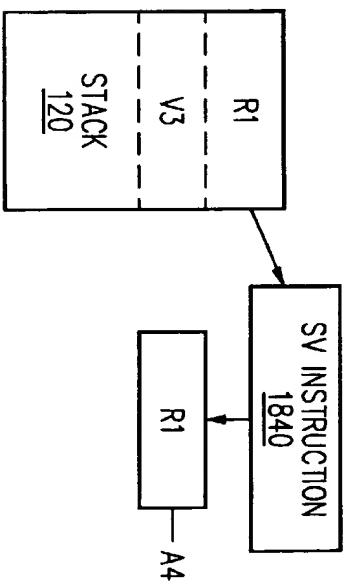


FIG. 18d

	Docum ent ID	U	Title	Current OR
106	US 57322 34 A	<input checked="" type="checkbox"/>	System for obtaining parallel execution of existing instructions in a particular data processing configuration by compounding rules based on instruction categories	712/200
107	US 57014 50 A	<input checked="" type="checkbox"/>	System including ATA sequencer microprocessor which executes sequencer instructions to handle plurality of real-time events allowing to perform all operations without local microprocessor intervention	712/245
108	US 57014 35 A	<input checked="" type="checkbox"/>	Instruction cache system for implementing programs having non-sequential instructions and method of implementing same	711/159
109	US 56853 96 A	<input checked="" type="checkbox"/>	Apparatus for automatically performing engine fluid changes	184/1.5
110	US 56849 72 A	<input checked="" type="checkbox"/>	Programmable servo burst sequencer for a disk drive	711/4
111	US 56780 48 A	<input checked="" type="checkbox"/>	Interrupt vector method and apparatus for loading a slot memory address counter	710/266
112	US 56405 83 A	<input checked="" type="checkbox"/>	Programmable servo burst decoder	713/600
113	US 56405 38 A	<input checked="" type="checkbox"/>	Programmable timing mark sequencer for a disk drive	703/23
114	US 56405 09 A	<input checked="" type="checkbox"/>	Programmable built-in self-test function for an integrated circuit	714/42
115	US 56319 74 A	<input checked="" type="checkbox"/>	Image processing	382/132
116	US 56128 34 A	<input checked="" type="checkbox"/>	Servo burst controller for a magnetic disk	360/75
117	US 56008 07 A	<input checked="" type="checkbox"/>	Programmable controller capable of updating a user program during operation by switching between user program memories	711/211
118	US 55967 37 A	<input checked="" type="checkbox"/>	Sequencer map for a hard disk controller combining data and next-address fields	711/213
119	US 55923 48 A	<input checked="" type="checkbox"/>	Method and structure for locating and skipping over servo bursts on a magnetic disk	360/77. 08
120	US 55726 66 A	<input checked="" type="checkbox"/>	System and method for generating pseudo-random instructions for design verification	714/32
121	US 55640 23 A	<input checked="" type="checkbox"/>	Method for accessing a sequencer control block by a host adapter integrated circuit	710/100
122	US 55621 81 A	<input checked="" type="checkbox"/>	Apparatus and method for automatically performing engine fluid changes	184/1.5
123	US 55599 76 A	<input checked="" type="checkbox"/>	System for instruction completion independent of result write-back responsive to both exception free completion of execution and completion of all logically prior instructions	712/215
124	US 55577 64 A	<input checked="" type="checkbox"/>	Interrupt vector method and apparatus	710/269
125	US 55533 01 A	<input checked="" type="checkbox"/>	Programmable sequencer having internal components which are microprocessor read/write interfactable	710/5
126	US 55487 93 A	<input checked="" type="checkbox"/>	System for controlling arbitration using the memory request signal types generated by the plurality of datapaths	710/40
127	US 55487 38 A	<input checked="" type="checkbox"/>	System and method for processing an instruction in a processing system	712/215

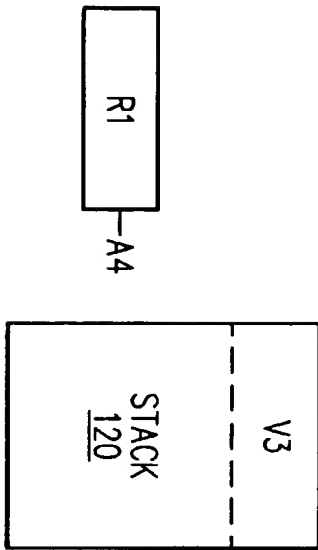


FIG. 18e

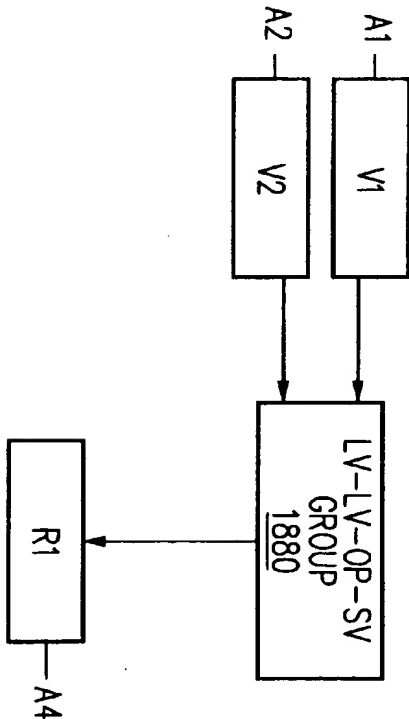


FIG. 18f

	Docum ent ID	U	Title	Current OR
128	US 55420 58 A	<input checked="" type="checkbox"/>	Pipelined computer with operand context queue to simplify context-dependent execution flow	713/502
129	US 55303 70 A	<input checked="" type="checkbox"/>	Testing apparatus for testing and handling a multiplicity of devices	324/754
130	US 55285 89 A	<input checked="" type="checkbox"/>	Distributed type packet switching system and a method of controlling a flow control execution	370/235
131	US 55265 00 A	<input checked="" type="checkbox"/>	System for operand bypassing to allow a one and one-half cycle cache memory access time for sequential load and branch instructions	712/218
132	US 55220 80 A	<input checked="" type="checkbox"/>	Centralized control SIMD processor having different priority levels set for each data transfer request type and successively repeating the servicing of data transfer request in a predetermined order	710/220
133	US 55176 65 A	<input checked="" type="checkbox"/>	System for controlling arbitration using the memory request signal types generated by the plurality of datapaths having dual-ported local memory architecture for simultaneous data transmission	712/9
134	US 55150 52 A	<input checked="" type="checkbox"/>	Universal remote control with function synthesis	341/176
135	US 55028 26 A	<input checked="" type="checkbox"/>	System and method for obtaining parallel existing instructions in a particular data processing configuration by compounding instructions	712/213
136	US 55009 42 A	<input checked="" type="checkbox"/>	Method of indicating parallel execution compoundability of scalar instructions based on analysis of presumed instructions	712/210
137	US 54993 50 A	<input checked="" type="checkbox"/>	Vector data processing system with instruction synchronization	712/220
138	US 54955 78 A	<input checked="" type="checkbox"/>	Apparatus and method for changing the behavior of a computer program while retaining control of program execution	714/51
139	US 54853 66 A	<input checked="" type="checkbox"/>	Sequence controller including error correction and method therefor	700/21
140	US 54737 63 A	<input checked="" type="checkbox"/>	Interrupt vector method and apparatus	712/244
141	US 54735 72 A	<input checked="" type="checkbox"/>	Power saving system for a memory controller	365/227
142	US 54695 72 A	<input checked="" type="checkbox"/>	Post compile optimizer for linkable object code	717/152
143	US 54674 68 A	<input checked="" type="checkbox"/>	Semiconductor memory device having built-in test circuits selectively activated by decoder circuit	714/726
144	US 54576 51 A	<input checked="" type="checkbox"/>	Method and architecture for accelerated programming of uniform data into an electrically programmable memory	365/185 .04
145	US 54521 01 A	<input checked="" type="checkbox"/>	Apparatus and method for decoding fixed and variable length encoded data	382/234
146	US 54487 46 A	<input checked="" type="checkbox"/>	System for comounding instructions in a byte stream prior to fetching and identifying the instructions for execution	712/210
147	US 54308 54 A	<input checked="" type="checkbox"/>	Simd with selective idling of individual processors based on stored conditional flags, and with consensus among all flags used for conditional branching	712/236
148	US 54288 02 A	<input checked="" type="checkbox"/>	Method and apparatus for executing critical disk access commands	710/9
149	US 54127 84 A	<input checked="" type="checkbox"/>	Apparatus for parallelizing serial instruction sequences and creating entry points into parallelized instruction sequences at places other than beginning of particular parallelized instruction sequence	712/245

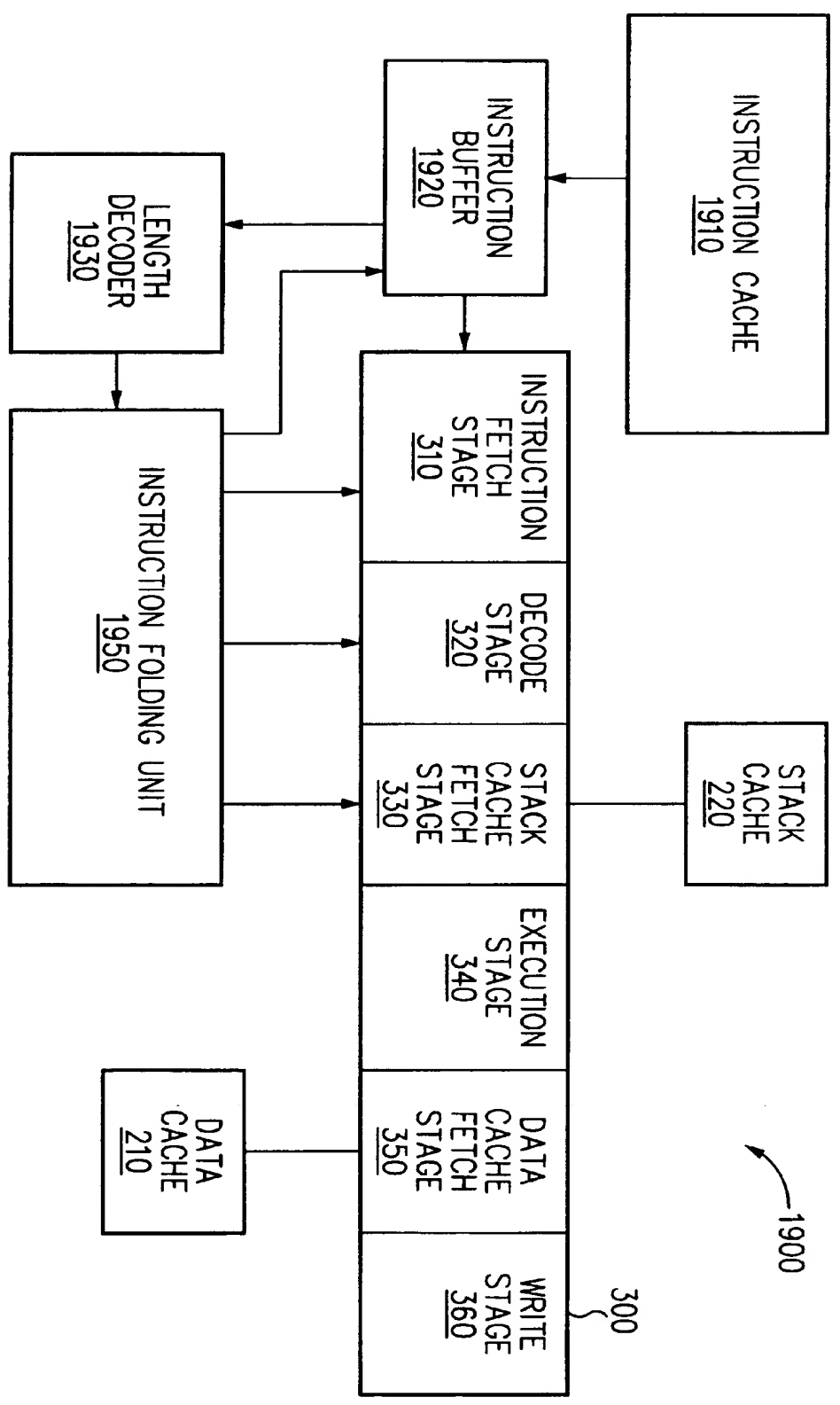


FIG. 19



	Docum ent ID	U	Title	Current OR
150	US 54086 58 A	<input checked="" type="checkbox"/>	Self-scheduling parallel computer system and method	712/216
151	US 53945 29 A	<input checked="" type="checkbox"/>	Branch prediction unit for high-performance processor	712/240
152	US 53879 28 A	<input checked="" type="checkbox"/>	Electronic endoscope system having both still and moving images	348/70
153	US 53814 19 A	<input checked="" type="checkbox"/>	Method and apparatus for detecting retention faults in memories	714/720
154	US 53632 96 A	<input checked="" type="checkbox"/>	Electronic cash register having macro-keys	705/18
155	US 53476 39 A	<input checked="" type="checkbox"/>	Self-parallelizing computer system and method	712/203
156	US 53332 96 A	<input checked="" type="checkbox"/>	Combined queue for invalidates and return data in multiprocessor system	711/171
157	US 53177 20 A	<input checked="" type="checkbox"/>	Processor system with writeback cache using writeback and non writeback transactions stored in separate queues	711/143
158	US 53075 04 A	<input checked="" type="checkbox"/>	System and method for preserving instruction granularity when translating program code from a computer having a first architecture to a computer having a second reduced architecture during the occurrence of interrupts due to asynchronous events	712/41
159	US 52631 53 A	<input checked="" type="checkbox"/>	Monitoring control flow in a microprocessor	714/51
160	US 52611 13 A	<input checked="" type="checkbox"/>	Apparatus and method for single operand register array for vector and scalar data processing operations	712/8
161	US 52531 86 A	<input checked="" type="checkbox"/>	Process facility monitoring method including transformation of sequential conditions into constraining conditions	702/182
162	US 52394 76 A	<input checked="" type="checkbox"/>	Multi-level state language controller for multi-threaded machine control	700/159
163	US 52187 12 A	<input checked="" type="checkbox"/>	Providing a data processor with a user-mode accessible mode of operations in which the processor performs processing operations without interruption	710/261
164	US 52028 89 A	<input checked="" type="checkbox"/>	Dynamic process for the generation of biased pseudo-random test patterns for the functional verification of hardware designs	714/739
165	US 51858 71 A	<input checked="" type="checkbox"/>	Coordination of out-of-sequence fetching between multiple processors using re-execution of instructions	712/205
166	US 51855 74 A	<input checked="" type="checkbox"/>	NMR measurements using recursive RF excitation	324/309
167	US 51670 35 A	<input checked="" type="checkbox"/>	Transferring messages between nodes in a network	714/4
168	US 51558 43 A	<input checked="" type="checkbox"/>	Error transition mode for multi-processor system	714/5
169	US 51509 77 A	<input checked="" type="checkbox"/>	Recording apparatus with detector for paper edge and end of ribbon sensing	400/703
170	US 51504 69 A	<input checked="" type="checkbox"/>	System and method for processor pipeline control by selective signal deassertion	712/244
171	US 51146 81 A	<input checked="" type="checkbox"/>	Superfusion apparatus	422/111

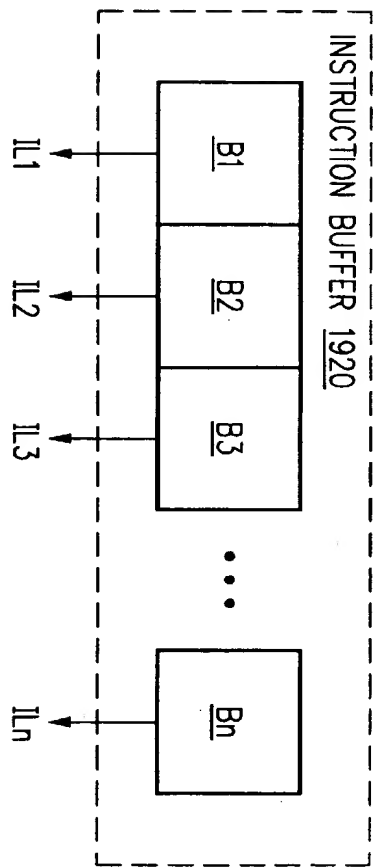


FIG. 20

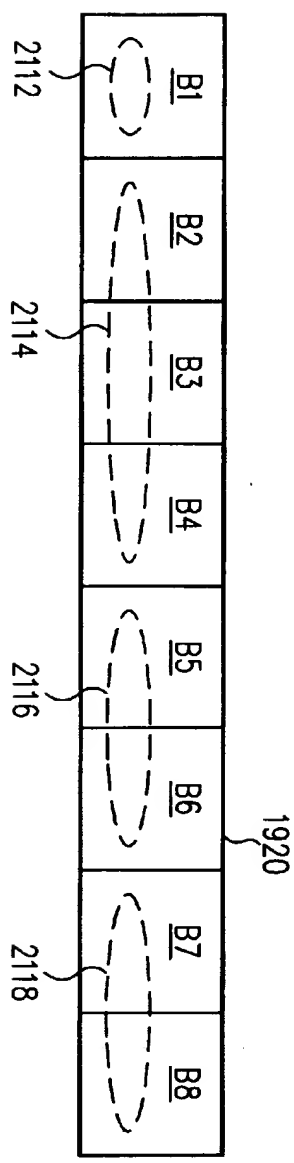


FIG. 21

	Docum ent ID	U	Title	Current OR
172	US 51135 15 A	<input checked="" type="checkbox"/>	Virtual instruction cache system using length responsive decoded instruction shifting and merging with prefetch buffer outputs to fill instruction buffer	711/125
173	US 50880 48 A	<input checked="" type="checkbox"/>	Massively parallel propositional reasoning	706/51
174	US 50581 14 A	<input checked="" type="checkbox"/>	Program control apparatus incorporating a trace function	714/38
175	US 50237 28 A	<input checked="" type="checkbox"/>	Image forming apparatus	358/437
176	US 49891 72 A	<input checked="" type="checkbox"/>	Apparatus and method for checking start signals	708/530
177	US 49568 00 A	<input checked="" type="checkbox"/>	Arithmetic operation processing apparatus of the parallel processing type and compiler which is used in this apparatus	708/524
178	US 49567 70 A	<input checked="" type="checkbox"/>	Method and device to execute two instruction sequences in an order determined in advance	712/220
179	US 49530 78 A	<input checked="" type="checkbox"/>	Apparatus and method for multi-threaded program execution in a microcoded data processing system	712/248
180	US 49473 69 A	<input checked="" type="checkbox"/>	Microword generation mechanism utilizing a separate branch decision programmable logic array	712/234
181	US 49439 16 A	<input checked="" type="checkbox"/>	Information processing apparatus for a data flow computer	712/26
182	US 49263 23 A	<input checked="" type="checkbox"/>	Streamlined instruction processor	712/238
183	US 49263 08 A	<input checked="" type="checkbox"/>	Programmable machine system	700/18
184	US 49166 02 A	<input checked="" type="checkbox"/>	Microcode control system in a microcomputer capable of branching to different microcode routines	712/245
185	US 48687 45 A	<input checked="" type="checkbox"/>	Data processing system and method for the direct and indirect execution of uniformly structured object types	711/202
186	US 48687 35 A	<input checked="" type="checkbox"/>	Interruptible structured microprogrammed sixteen-bit address sequence controller	712/234
187	US 48538 89 A	<input checked="" type="checkbox"/>	Arrangement and method for speeding the operation of branch instructions	712/237
188	US 48112 11 A	<input checked="" type="checkbox"/>	On-line overflow response system and ALU branching structure	708/525
189	US 48021 16 A	<input checked="" type="checkbox"/>	Programmed controller	703/23
190	US 47424 53 A	<input checked="" type="checkbox"/>	Pipeline-controlled information processing system for generating updated condition code	712/234
191	US 47195 65 A	<input checked="" type="checkbox"/>	Interrupt and trap handling in microprogram sequencer	710/260
192	US 46959 83 A	<input checked="" type="checkbox"/>	Calculator or pocket computer with selectable operational sequence	708/144
193	US 46895 64 A	<input checked="" type="checkbox"/>	Digital interface subsystem for a magnetic resonance imaging and spectroscopy system	324/309
194	US 45861 27 A	<input checked="" type="checkbox"/>	Multiple control stores for a pipelined microcontroller	712/243

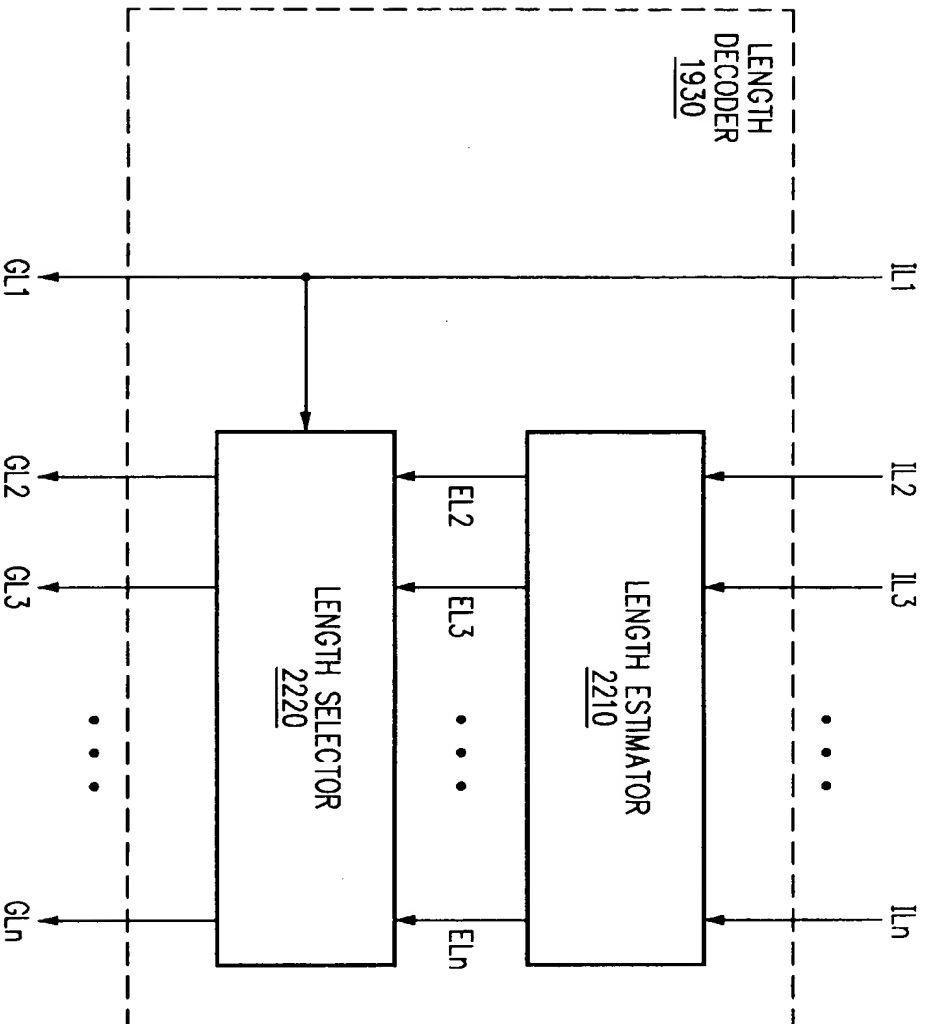


FIG. 22

	Docum ent ID	U	Title	Current OR
195	US 45758 16 A	<input checked="" type="checkbox"/>	Interactive transactions processor using sequence table pointers to access function table statements controlling execution of specific interactive functions	345/853
196	US 45517 98 A	<input checked="" type="checkbox"/>	Multiple control stores in a pipelined microcontroller for handling nester subroutines	712/243
197	US 45478 60 A	<input checked="" type="checkbox"/>	Computer keyboards with few keys designating hundreds of functions	708/146
198	US 45464 31 A	<input checked="" type="checkbox"/>	Multiple control stores in a pipelined microcontroller for handling jump and return subroutines	712/243
199	US 45218 50 A	<input checked="" type="checkbox"/>	Instruction buffer associated with a cache memory unit	712/200
200	US 45035 28 A	<input type="checkbox"/>	Method and apparatus for controlling vehicle mounted devices and equipment	367/198

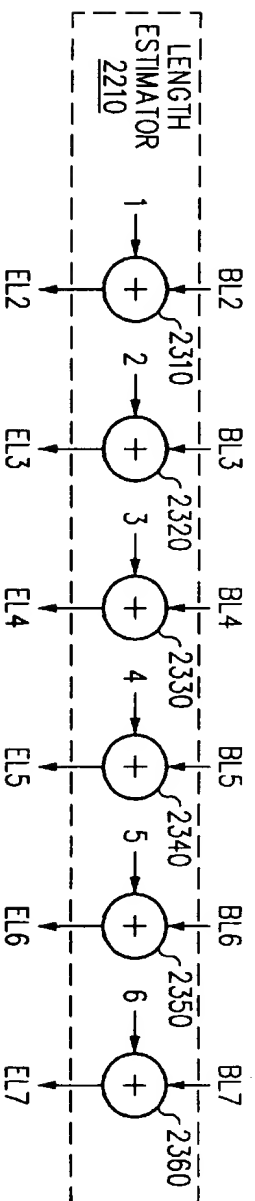


FIG. 23

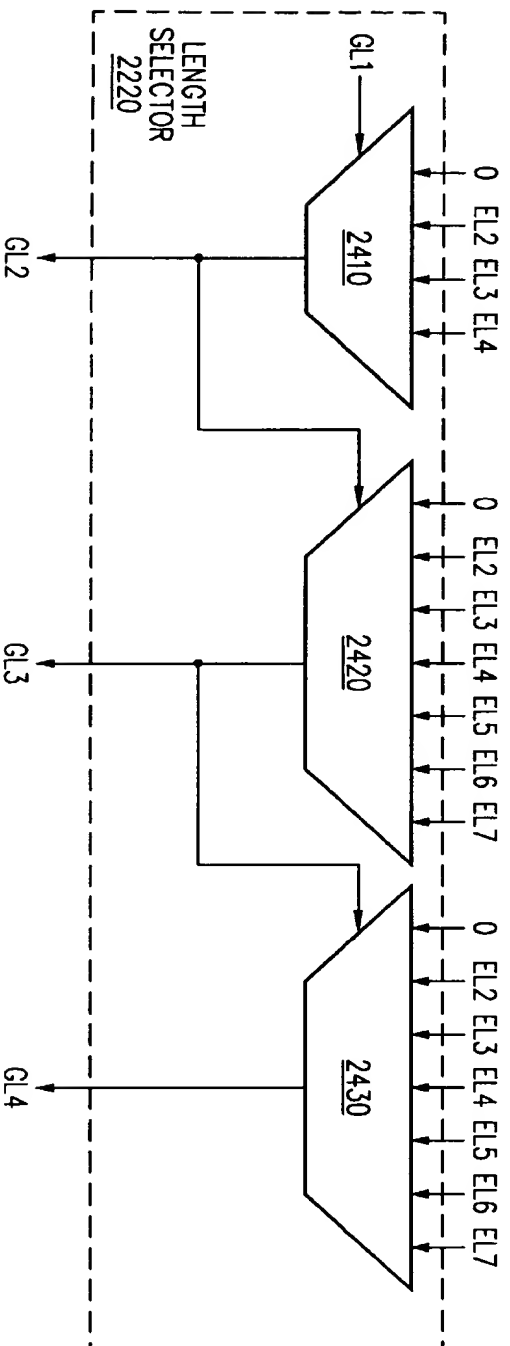


FIG. 24

	L #	Hits	Search Text	DBs
1	L1	93761	(speculative\$3 sequen\$4 order) near10 (instruction execut\$3)	USPAT; US-PGPUB
2	L2	1692	(indicat\$3 flag tag bit field mode) near10 (allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near20 1	USPAT; US-PGPUB
3	L3	445	((speculative\$3 sequen\$4 order) and (instruction execut\$3)).ab,ti. and 2	USPAT; US-PGPUB
4	L8	95938	(speculative\$3 sequen\$4 order predict\$3) near10 (instruction execut\$3)	USPAT; US-PGPUB
5	L9	1793	(indicat\$3 flag tag bit field mode) near10 (allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near20 8	USPAT; US-PGPUB
6	L10	527	((speculative\$3 sequen\$4 order predict\$3) and (instruction execut\$3)).ab,ti. and 9	USPAT; US-PGPUB
7	L11	31579	(speculative\$3 sequen\$4 order predict\$3) near10 (instruction execut\$3)	EPO; JPO; DERWENT; IBM_TDB
8	L12	157	(indicat\$3 flag tag bit field mode) near10 (allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near20 11	EPO; JPO; DERWENT; IBM_TDB
9	L13	62	9 near10 speculative\$3	USPAT; US-PGPUB
10	L19	95947	(speculat\$6 sequen\$4 order predict\$3) near10 (instruction execut\$3)	USPAT; US-PGPUB
11	L22	31612	(speculat\$6 sequen\$4 order predict\$3) near10 (instruction execut\$3)	EPO; JPO; DERWENT; IBM_TDB
12	L33	1734	(indicat\$3 flag tag bit field mode) near10 ((allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near10 19)	USPAT; US-PGPUB
13	L34	563	((speculat\$6 sequen\$4 order predict\$3 load) and (instruction execut\$3)).ab,ti. and 33	USPAT; US-PGPUB
14	L35	25	(indicat\$3 flag tag bit field mode) near10 ((allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near10 22) not 12	EPO; JPO; DERWENT; IBM_TDB
15	L36	56467	(speculat\$6 order predict\$3) near10 (instruction execut\$3)	USPAT; US-PGPUB
16	L37	273	(indicat\$3 flag tag bit field mode) near10 ((allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near10 36) and 34 not 13	USPAT; US-PGPUB
17	L38	243	34 not (37 13)	USPAT; US-PGPUB

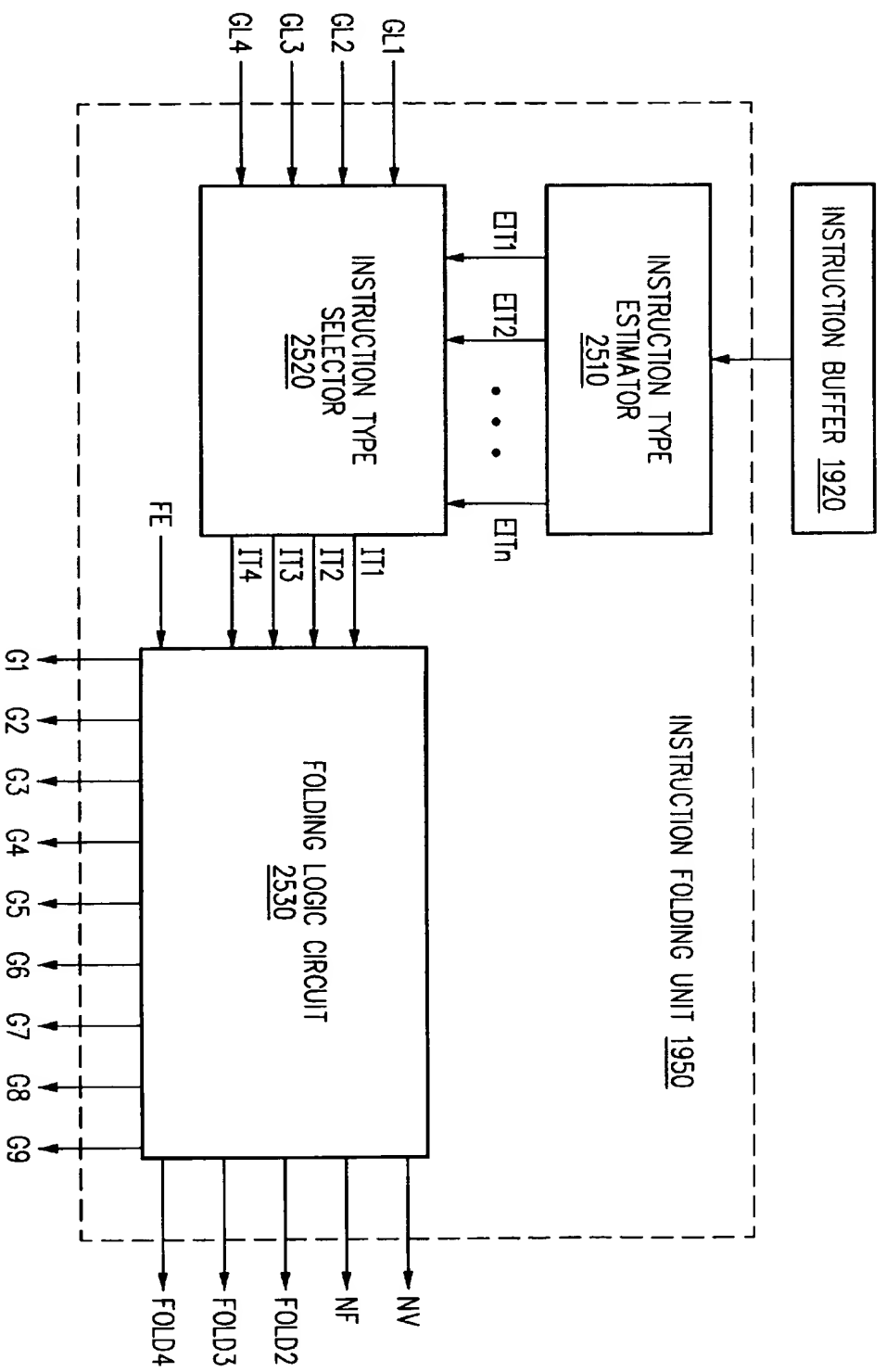


FIG. 25



	L #	Hits	Search Text	DBs
1	L1	93761	(speculative\$3 sequen\$4 order) near10 (instruction execut\$3)	USPAT; US-PGPUB
2	L2	1692	(indicat\$3 flag tag bit field mode) near10 (allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near20 1	USPAT; US-PGPUB
3	L3	445	((speculative\$3 sequen\$4 order) and (instruction execut\$3)).ab,ti. and 2	USPAT; US-PGPUB
4	L8	95938	(speculative\$3 sequen\$4 order predict\$3) near10 (instruction execut\$3)	USPAT; US-PGPUB
5	L9	1793	(indicat\$3 flag tag bit field mode) near10 (allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near20 8	USPAT; US-PGPUB
6	L10	527	((speculative\$3 sequen\$4 order predict\$3) and (instruction execut\$3)).ab,ti. and 9	USPAT; US-PGPUB
7	L11	31579	(speculative\$3 sequen\$4 order predict\$3) near10 (instruction execut\$3)	EPO; JPO; DERWENT; IBM_TDB
8	L12	157	(indicat\$3 flag tag bit field mode) near10 (allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near20 11	EPO; JPO; DERWENT; IBM_TDB
9	L13	62	9 near10 speculative\$3	USPAT; US-PGPUB
10	L19	95947	(speculat\$6 sequen\$4 order predict\$3) near10 (instruction execut\$3)	USPAT; US-PGPUB
11	L20	1797	(indicat\$3 flag tag bit field mode) near10 (allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near20 19	USPAT; US-PGPUB
12	L22	31612	(speculat\$6 sequen\$4 order predict\$3) near10 (instruction execut\$3)	EPO; JPO; DERWENT; IBM_TDB
13	L23	0	(indicat\$3 flag tag bit field mode) near10 (allow\$3 permit\$4 enabl\$3 disabl\$3 prohibit\$3 inhibit\$3 activ\$5 deactiv\$5) near20 22 not 12	EPO; JPO; DERWENT; IBM_TDB
14	L25	529	((speculat\$6 sequen\$4 order predict\$3) and (instruction execut\$3)).ab,ti. and 20	USPAT; US-PGPUB
15	L26	487	25 not 13	USPAT; US-PGPUB

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US006499098	20	1 - 20	1
US006330657	21	1 - 21	1
US005163139	12	1 - 12	1
Total (3)	53	-	-

	Docum ent ID	U	Title	Current OR
1	US 55600 32 A	<input type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution and concurrent results distribution	712/23
2	US 55600 25 A	<input checked="" type="checkbox"/>	Entry allocation apparatus and method of same	712/23
3	US 55554 28 A	<input checked="" type="checkbox"/>	Activity masking with mask context of SIMD processors	712/22
4	US 55532 55 A	<input checked="" type="checkbox"/>	Data processor with programmable levels of speculative instruction fetching and method of operation	712/235
5	US 55399 11 A	<input checked="" type="checkbox"/>	High-performance, superscalar-based computer system with out-of-order instruction execution	712/23
6	US 55308 15 A	<input checked="" type="checkbox"/>	Apparatus and method for verifying the order and operation of a data processing device when asynchronous commands are held in a command queue	712/227
7	US 55240 88 A	<input checked="" type="checkbox"/>	Multi-functional operating circuit providing capability of freely combining operating functions	708/493
8	US 55220 53 A	<input checked="" type="checkbox"/>	Branch target and next instruction address calculation in a pipeline processor	711/213
9	US 55070 28 A	<input checked="" type="checkbox"/>	History based branch prediction accessed via a history based earlier instruction address	712/207
10	US 55009 47 A	<input checked="" type="checkbox"/>	Operand specifier processing by grouping similar specifier types together and providing a general routine for each	712/211
11	US 54902 80 A	<input checked="" type="checkbox"/>	Apparatus and method for entry allocation for a resource buffer	712/23
12	US 54817 44 A	<input checked="" type="checkbox"/>	Microcode sequencer changing states in response to an external gating input level change upon the occurrence of a wait instruction	712/227
13	US 54816 79 A	<input checked="" type="checkbox"/>	Data processing apparatus having bus switches for selectively connecting buses to improve data throughput	710/316
14	US 54715 93 A	<input checked="" type="checkbox"/>	Computer processor with an efficient means of executing many instructions simultaneously	712/235
15	US 54653 61 A	<input checked="" type="checkbox"/>	Microcode linker/loader that generates microcode sequences for MRI sequencer by modifying previously generated microcode sequences	717/168
16	US 54634 32 A	<input checked="" type="checkbox"/>	Miniature pan/tilt tracking mount	352/243
17	US 54541 17 A	<input checked="" type="checkbox"/>	Configurable branch prediction for a processor performing speculative execution	712/23
18	US 54540 86 A	<input checked="" type="checkbox"/>	Dynamic program analyzer facility	712/227
19	US 54540 77 A	<input checked="" type="checkbox"/>	Communication system between a plurality of transmitters and receivers having relays responsive to those identifying codes of transmitters contained in its respective table memory	710/106
20	US 54487 05 A	<input checked="" type="checkbox"/>	RISC microprocessor architecture implementing fast trap and exception state	712/244
21	US 54434 27 A	<input checked="" type="checkbox"/>	Apparatus for controlling automatic transmission	475/123
22	US 54370 48 A	<input checked="" type="checkbox"/>	Programmable controller acting as a master station and having automatic control of interlock process by using an operation complete address flag	709/208
23	US 54148 22 A	<input checked="" type="checkbox"/>	Method and apparatus for branch prediction using branch prediction table with improved branch prediction effectiveness	712/240

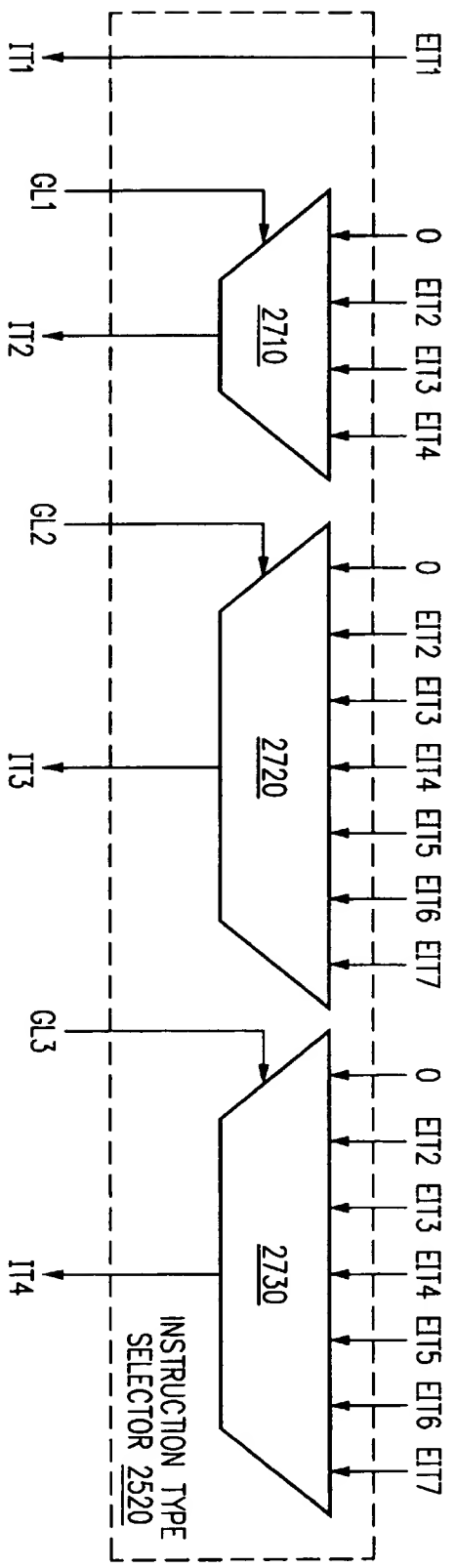


FIG. 27

	Docum ent ID	U	Title	Current OR
24	US 53136 44 A	<input checked="" type="checkbox"/>	System having status update controller for determining which one of parallel operation results of execution units is allowed to set conditions of shared processor status word	712/228
25	US 52952 48 A	<input checked="" type="checkbox"/>	Branch control circuit	712/239
26	US 52916 10 A	<input checked="" type="checkbox"/>	Microcode sequencer changing states in response to an external gating input level change upon the occurrence of a WAIT instruction	712/226
27	US 52874 67 A	<input checked="" type="checkbox"/>	Pipeline for removing and concurrently executing two or more branch instructions in synchronization with other instructions executing in the execution unit	712/235
28	US 52476 93 A	<input checked="" type="checkbox"/>	Computer language structure for process control applications and method of translating same into program code to operate the computer	717/139
29	US 52281 31 A	<input checked="" type="checkbox"/>	Data processor with selectively enabled and disabled branch prediction operation	712/240
30	US 52069 38 A	<input checked="" type="checkbox"/>	IC card with memory area protection based on address line restriction	711/200
31	US 51931 56 A	<input checked="" type="checkbox"/>	Data processor with pipeline which disables exception processing for non-taken branches	712/239
32	US 51685 66 A	<input checked="" type="checkbox"/>	Multi-task control device for central processor task execution control provided as a peripheral device and capable of prioritizing and timesharing the tasks	718/103
33	US 51596 76 A	<input checked="" type="checkbox"/>	Semi-smart DRAM controller IC to provide a pseudo-cache mode of operation using standard page mode draws	711/107
34	US 51442 42 A	<input checked="" type="checkbox"/>	Continually loadable microcode store for MRI control sequencers	324/312
35	US 51013 53 A	<input checked="" type="checkbox"/>	Automated system for providing liquidity to securities markets	705/37
36	US 51013 41 A	<input checked="" type="checkbox"/>	Pipelined system for reducing instruction access time by accumulating predecoded instruction bits a FIFO	712/213
37	US 50815 74 A	<input checked="" type="checkbox"/>	Branch control in a three phase pipelined signal processor	712/234
38	US 50723 64 A	<input checked="" type="checkbox"/>	Method and apparatus for recovering from an incorrect branch prediction in a processor that executes a family of instructions in parallel	712/215
39	US 50088 07 A	<input checked="" type="checkbox"/>	Data processing apparatus with abbreviated jump field	712/213
40	US 49396 44 A	<input checked="" type="checkbox"/>	Input/output controller for controlling the sequencing of the execution of input/output commands in a data processing system	710/5
41	US 49012 32 A	<input checked="" type="checkbox"/>	I/O controller for controlling the sequencing of execution of I/O commands and for permitting modification of I/O controller operation by a host processor	710/6
42	US 48705 73 A	<input checked="" type="checkbox"/>	Microcomputer capable of testing execution of a program with no branch	714/38
43	US 48687 40 A	<input checked="" type="checkbox"/>	System for processing data with multiple virtual address and data word lengths	711/2
44	US 48601 99 A	<input checked="" type="checkbox"/>	Hashing indexer for branch cache	711/213
45	US 48581 04 A	<input checked="" type="checkbox"/>	Preceding instruction address based branch prediction in a pipelined processor	712/240
46	US 48538 40 A	<input checked="" type="checkbox"/>	Instruction prefetching device including a circuit for checking prediction of a branch instruction before the instruction is executed	712/237

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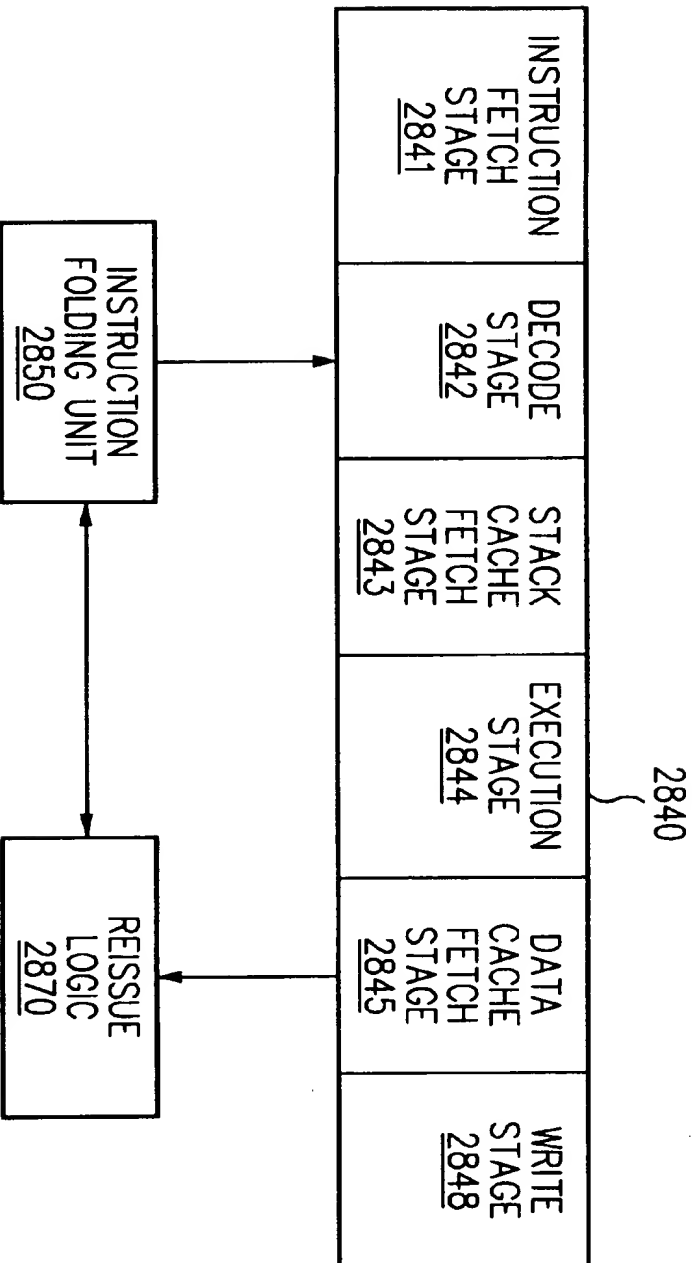


FIG. 28

	Docum ent ID	U	Title	Current OR
47	US 47945 17 A	<input checked="" type="checkbox"/>	Three phased pipelined signal processor	712/32
48	US 47853 93 A	<input checked="" type="checkbox"/>	32-Bit extended function arithmetic-logic unit on a single chip	712/221
49	US 47775 94 A	<input checked="" type="checkbox"/>	Data processing apparatus and method employing instruction flow prediction	712/240
50	US 47605 19 A	<input checked="" type="checkbox"/>	Data processing apparatus and method employing collision detection and prediction	712/217
51	US 47559 35 A	<input checked="" type="checkbox"/>	Prefetch memory system having next-instruction buffer which stores target tracks of jumps prior to CPU access of instruction	712/233
52	US 47501 12 A	<input checked="" type="checkbox"/>	Data processing apparatus and method employing instruction pipelining	712/217
53	US 47413 11 A	<input checked="" type="checkbox"/>	Method of air/fuel ratio control for internal combustion engine	123/675
54	US 47363 20 A	<input checked="" type="checkbox"/>	Computer language structure for process control applications, and translator therefor	717/109
55	US 46881 88 A	<input checked="" type="checkbox"/>	Data storage apparatus for storing groups of data with read and write request detection	711/114
56	US 46723 60 A	<input checked="" type="checkbox"/>	Apparatus and method for converting a number in binary format to a decimal format	341/104
57	US 45946 61 A	<input checked="" type="checkbox"/>	Microword control system utilizing multiplexed programmable logic arrays	712/248
58	US 45576 94 A	<input checked="" type="checkbox"/>	Teaching device and method of using same	434/339
59	US 44843 00 A	<input checked="" type="checkbox"/>	Data processor having units carry and tens carry apparatus supporting a decimal multiply operation	708/623
60	US 44620 73 A	<input checked="" type="checkbox"/>	Apparatus for fetching and decoding instructions	712/207
61	US 44569 94 A	<input checked="" type="checkbox"/>	Remote simulation by remote control from a computer desk	714/33
62	US 44478 77 A	<input checked="" type="checkbox"/>	Memory bus interface system	713/502
63	US 44307 06 A	<input checked="" type="checkbox"/>	Branch prediction apparatus and method for a data processing system	712/237
64	US 44266 80 A	<input checked="" type="checkbox"/>	Data processor using read only memories for optimizing main memory access and identifying the starting position of an operand	711/214
65	US 43843 41 A	<input checked="" type="checkbox"/>	Data processor having carry apparatus supporting a decimal divide operation	708/652
66	US 43162 44 A	<input checked="" type="checkbox"/>	Memory apparatus for digital computer system	711/168
67	US 42478 94 A	<input checked="" type="checkbox"/>	Arrangement for program interruption	710/264
68	US 40400 21 A	<input checked="" type="checkbox"/>	Circuit for increasing the apparent occupancy of a processor	713/601
69	US 40370 94 A	<input checked="" type="checkbox"/>	Multi-functional arithmetic and logical unit	708/231

2900

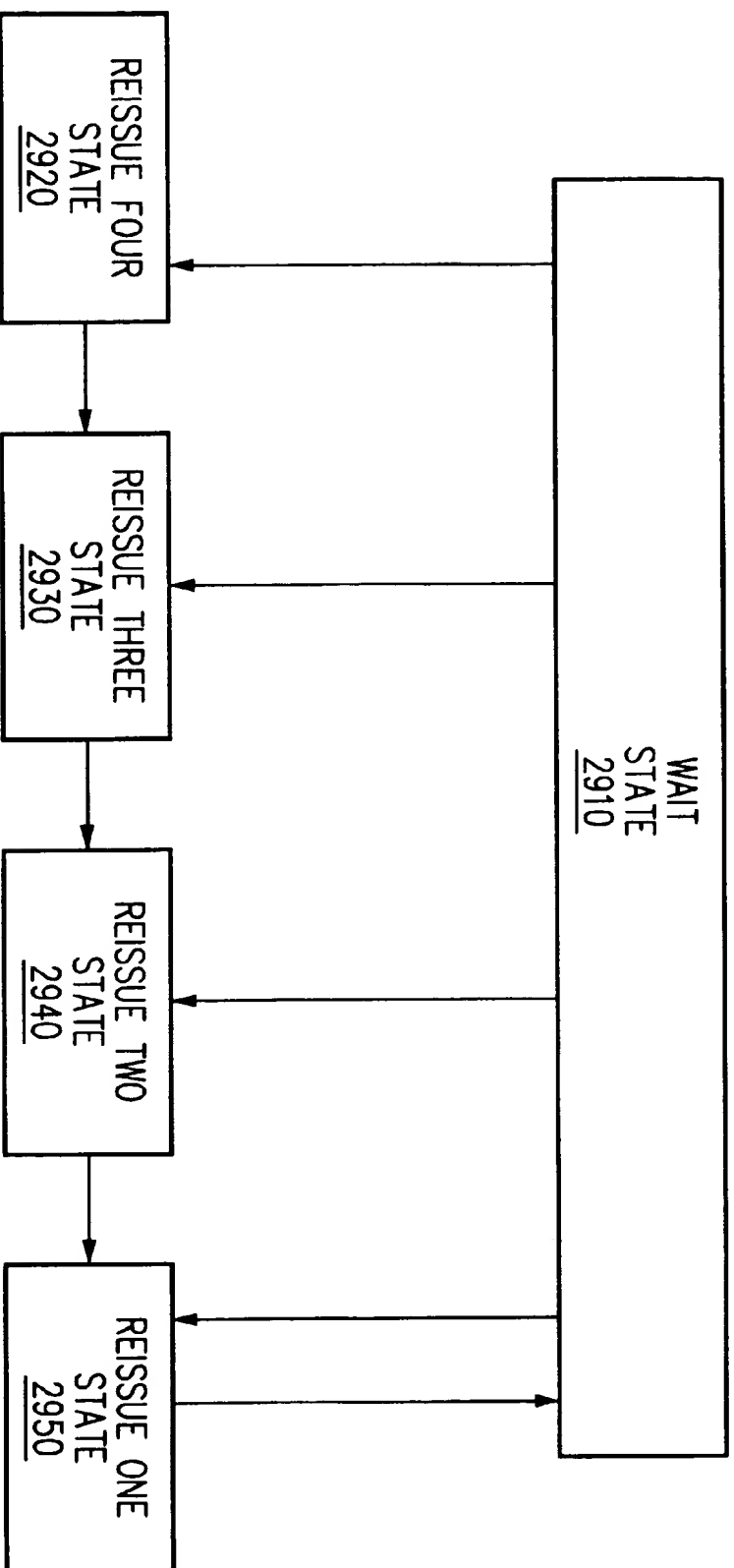


FIG. 29



	Docum ent ID	U	Title	Current OR
70	US 39626 84 A	<input checked="" type="checkbox"/>	Computing system interface using common parallel bus and segmented addressing	710/100
71	US 39626 83 A	<input checked="" type="checkbox"/>	CPU programmable control system	713/600
72	US 38259 03 A	<input checked="" type="checkbox"/>	AUTOMATIC SWITCHING OF STORAGE PROTECT KEYS	711/163
73	US 37573 06 A	<input checked="" type="checkbox"/>	COMPUTING SYSTEMS CPU	712/32
74	US 37365 67 A	<input checked="" type="checkbox"/>	PROGRAM SEQUENCE CONTROL	712/231

# LENGTH DECODER FOR VARIABLE LENGTH DATA

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application relates to the co-pending application Ser. No. 09/064,807, filed Apr. 22, 1998, "SUPERSCALAR STACK BASED COMPUTING SYSTEM", by Koppala, et al. owned by the assignee of this application and incorporated herein by reference.

This application relates to the co-pending application Ser. No. 09/064,682, filed Apr. 22, 1998, "REISSUE LOGIC FOR HANDLING TRAPS IN A MULTISSUE STACK BASED COMPUTING SYSTEM", by Koppala, et al. owned by the assignee of this application and incorporated herein by reference.

1. Field of the Invention

The present invention relates generally to computing systems and, in particular, to super-scalar stack based computing systems.

However, other memory architectures such as stacks are also used in computing systems. As shown in FIG. 1, a stack based computing system 110, which can implement for example, the JAVA Virtual Machine, is coupled to a stack 120. In classical stack architectures, data is either "pushed" onto the stack or "popped" off the stack by stack based computing system 110. For example, to add the numbers 4 and 5, a stack based computing system 110 first pushes the number 4 onto the top of stack 120. Then, stack based computing system 110 pushes the number 5 onto the stack. Then, stack based computing system 110 performs an add operation which pops the number 5 off stack 120 and the number 4 off stack 120 and pushes the number 9 onto the top of stack 120. A major advantage of stack based computing system 110 is that operations using data at the top of the stack do not need to use memory addresses. The top of stack 120 is also referred to as the first location of the stack, and the location just under the top of the stack is also referred to as the second location of the stack. Similarly, the memory location in the stack just after the second location is also referred to as the third location of the stack.

Stack based computing system 110 can become more flexible by also allowing stack based computing system 110 to use some random access techniques with stack 120. Thus, in some implementation of stack based computing system 110 and stack 120, the memory locations in stack 120 are part of a random-access memory architecture. Thus, each memory location in stack 120 has a memory address. As

used herein, a memory location having a memory address equal to x is referred to as memory location x.

Even in stack based computing systems using random-access techniques by the stack based computing system 110, most operations use data from or near the top of stack 120. For example, assume a value V1 from a memory location ADDR1 is to be added to a value V2 from a memory location ADDR2, and the sum stored at a memory location ADDR3, stack based computing system 110 first retrieves value V1 from stack 120, which retrieves value V1 from memory location ADDR1 and pushes value V1 onto the top of stack 120. Next, stack based computing system 110 executes another stack load instruction, which retrieves value V2 from memory location ADDR2 and pushes value V2 onto the top of stack 120. Then, stack based computing system 110 executes an add instruction which pops the top two locations of stack 120, which now contain value V1 and value V2, and pushes the sum of value V1 and value V2 onto the top of stack 120. Finally, stack based computing system 110 executes a stack store instruction which pops the value from the top of stack 120, i.e. the sum of value V1 and value V2, and stores the value in memory location ADDR3.

Some of the techniques used to improve the performance of random access memory systems can be adapted to improve stack performance. For example, as shown in FIG. 2, stack 120 can contain a data cache 210, a stack cache 220, a stack cache management unit 240, and a memory circuit 230. Data cache 210 is formed with fast memory circuits, such as SRAMS, to improve the throughput of memory circuit 230. Stack cache 220 specifically caches a top portion of stack 120 using fast memory circuits, such as SRAMS. Stack cache management unit 240 manages stack cache 220 by copying data from memory circuit 230 into stack cache 220 as data is popped off of stack 120 or spilling data from stack cache 220 to memory circuit 230 as data is pushed onto stack 120. Thus, stack cache 220 maintains the top of stack 120 in fast memory circuit, so that a stack based computing system can perform stack operations with low stack latency. Specific implementations of stack caches and stack management units are described in U.S. patent application Ser. No. 08/828,899, entitled "Stack Caching Circuit with Overflow/Underflow unit", by Sailerendra Koppala, which is hereby incorporated by reference.

Once stack latency is reduced, the operating speed of a stack based computing system may be limited by the rate at which stack operations can be performed. In general-purpose processing units, such as RISC microprocessors, pipelining and super-scalar implementation are used to improve the performance of the processing units. However, the techniques used for RISC processors are not easily adapted to stack based computing systems. For example, in super-scalar architectures, data dependencies determine which instructions can be issued simultaneously. However, for stack based computing systems, most stack operations use the top of the stack and would thus have a data dependency conflict. Hence, there is a need for a stack based computing system architecture to improve the performance of stack based computing systems.

Accordingly, the present invention provides pipelining techniques to prevent pipeline stalls and a super-scalar architecture for stack based computing systems, which can issue multiple stack operations concurrently. In accordance with one embodiment of the present invention, a stack based computing system includes an instruction pipeline, which

## SUMMARY

used herein, a memory location having a memory address equal to x is referred to as memory location x.

	Docum ent ID	U	Title	Current OR
1	US 20030 16729 2 A1	<input type="checkbox"/>	Method and apparatus for performing critical tasks using speculative operations	718/101
2	US 20030 10133 5 A1	<input type="checkbox"/>	Method for binary-level branch reversal on computer architectures supporting predicated execution	712/234
3	US 20030 08875 9 A1	<input type="checkbox"/>	System and method to reduce execution of instructions involving unreliable data in a speculative processor	712/218
4	US 20030 03351 0 A1	<input type="checkbox"/>	Methods and apparatus for controlling speculative execution of instructions based on a multiaccess memory condition	712/235
5	US 20020 19446 4 A1	<input type="checkbox"/>	Speculative branch target address cache with selective override by secondary predictor based on branch instruction type	712/239
6	US 20020 19446 3 A1	<input type="checkbox"/>	Speculative hybrid branch direction predictor	712/239
7	US 20020 19446 2 A1	<input type="checkbox"/>	Apparatus and method for selecting one of multiple target addresses stored in a speculative branch target address cache per instruction cache line	712/238
8	US 20020 19446 1 A1	<input type="checkbox"/>	Speculative branch target address cache	712/238
9	US 20020 19446 0 A1	<input type="checkbox"/>	Apparatus, system and method for detecting and correcting erroneous speculative branch target address cache branches	712/238
10	US 20020 18883 4 A1	<input type="checkbox"/>	Apparatus and method for target address replacement in speculative branch target address cache	712/238
11	US 20020 18883 3 A1	<input type="checkbox"/>	Dual call/return stack branch prediction system	712/236
12	US 20020 09200 2 A1	<input type="checkbox"/>	Method and apparatus for preserving precise exceptions in binary translated code	717/137
13	US 20020 06600 5 A1	<input type="checkbox"/>	Data processor with an improved data dependence detector	712/218
14	US 20010 00475 7 A1	<input type="checkbox"/>	Processor and method of controlling the same	712/218
15	US 66315 14 B1	<input type="checkbox"/>	Emulation system that uses dynamic binary translation and permits the safe speculation of trapping operations	717/137
16	US 66292 38 B1	<input type="checkbox"/>	Predicate controlled software pipelined loop processing with prediction of predicate writing and value prediction for use in subsequent iteration	712/241
17	US 66222 35 B1	<input type="checkbox"/>	Scheduler which retries load/store hit situations	712/23
18	US 66153 40 B1	<input type="checkbox"/>	Extended operand management indicator structure and method	712/209

instructions.

8. The digital computer system as in claim 7 wherein means coupling said input means of said instruction compounding mechanism to an output of said larger-capacity, lower-speed storage mechanism for transferring instructions from said larger-capacity, lower-speed storage mechanism to said instruction compounding mechanism transfers said instructions in unmodified object code.

9. The combination of claim 8 wherein the instruction compounding mechanism includes:

10 a plural-instruction instruction register for receiving a plurality of successive instructions from the lower-speed storage mechanism;

15 a plurality of rule-based instruction analyzer mechanisms, each of which analyzes a different pair of side-by-side instructions; the instruction register and includes means for producing a compoundability signal which indicates whether or not the two instructions in its pair may be processed in parallel;

20 and a tag generating mechanism responsive to the compoundability signals for generating the individual tag fields for the analyzed instructions in the instruction register.

10. The combination of claim 9 wherein:

25 the computer system has a particular instruction processing configuration having a plurality of functional units of one or more types;

and each instruction analyzer mechanism includes logic circuitry for implementing rules which define which types of instructions are compatible for parallel execution in the particular instruction processing configuration used for the computer system, such logic circuitry providing said means for producing the compoundability signal for that analyzer mechanism.

11. The digital computer system as in claim 1, wherein the instruction compounding mechanism includes:

35 a plural-instruction instruction register for receiving a plurality of successive instructions from the lower-speed storage mechanism;

40 a plurality of rule-based instruction analyzer mechanisms,

each of which analyzes a different pair of side-by-side instructions with unmodified object code in the instruction register and produces a compoundability signal which indicates whether or not the two instructions in its pair may be processed in parallel; and

45 a tag generating mechanism responsive to the compoundability signals for generating the individual tag fields for the different instructions of unmodified object code in the instruction register.

12. The combination of claim 1 wherein:

50 the computer system has a particular instruction processing configuration;

and each instruction analyzer mechanism includes logic circuitry for implementing rules which define which types of instructions are compatible for parallel execution in the particular instruction processing configuration used for the computer system, such logic circuitry producing the compoundability signal for that analyzer mechanism.

13. The digital computer system as in claim 1, wherein means coupling said input means of said instruction compounding mechanism to an output of said larger-capacity, lower-speed storage mechanism for transferring instructions from said larger-capacity, lower-speed storage mechanism to said instruction compounding mechanism transfers said instructions in unmodified object code.

14. The digital computer system as in claim 1 wherein said data bits indicating parallel execution of said instruction pairs comprise a binary data bit associated with each instruction, said binary data bit indicating in one of its states that an associated instruction is a first instruction of a compoundable pair of instructions and said binary data bit indicating in its other state that an associated instruction is a second instruction of a compoundable pair of instructions, a pair of instructions indicated as compoundable only when a binary data bit associated with a first instruction is in said one state and a binary data bit associated with a second instruction is in said other state.

	Docum ent ID	U	Title	Current OR
19	US 66091 91 B1	<input type="checkbox"/>	Method and apparatus for speculative microinstruction pairing	712/216
20	US 65780 59 B1	<input type="checkbox"/>	Methods and apparatus for controlling exponent range in floating-point calculations	708/496
21	US 65643 15 B1	<input type="checkbox"/>	Scheduler which discovers non-speculative nature of an instruction after issuing and reissues the instruction	712/214
22	US 65429 84 B1	<input type="checkbox"/>	Scheduler capable of issuing and reissuing dependency chains	712/214
23	US 65359 73 B1	<input type="checkbox"/>	Method and system for speculatively issuing instructions	712/218
24	US 63706 39 B1	<input type="checkbox"/>	Processor architecture having two or more floating-point status fields	712/222
25	US 63112 61 B1	<input type="checkbox"/>	Apparatus and method for improving superscalar processors	712/23
26	US 62125 39 B1	<input type="checkbox"/>	Methods and apparatus for handling and storing bi-endian words in a floating-point processor	708/495
27	US 61759 10 B1	<input type="checkbox"/>	Speculative instructions execution in VLIW processors	712/217
28	US 61516 69 A	<input type="checkbox"/>	Methods and apparatus for efficient control of floating-point status register	712/222
29	US 61120 19 A	<input type="checkbox"/>	Distributed instruction queue	712/214
30	US 60981 67 A	<input type="checkbox"/>	Apparatus and method for fast unified interrupt recovery and branch recovery in processors supporting out-of-order execution	712/218
31	US 60527 76 A	<input type="checkbox"/>	Branch operation system where instructions are queued until preparations is ascertained to be completed and branch distance is considered as an execution condition	712/233
32	US 60386 57 A	<input type="checkbox"/>	Scan chains for out-of-order load/store execution control	712/216
33	US 60322 45 A	<input type="checkbox"/>	Method and system for interrupt handling in a multi-processor computer system executing speculative instruction threads	712/23
34	US 60322 44 A	<input type="checkbox"/>	Multiple issue static speculative instruction scheduling with path tag and precise interrupt handling	712/23
35	US 59833 36 A	<input type="checkbox"/>	Method and apparatus for packing and unpacking wide instruction word using pointers and masks to shift word syllables to designated execution units groups	712/24
36	US 59665 30 A	<input type="checkbox"/>	Structure and method for instruction boundary machine state restoration	712/244
37	US 59580 48 A	<input type="checkbox"/>	Architectural support for software pipelining of nested loops	712/241
38	US 59266 46 A	<input type="checkbox"/>	Context-dependent memory-mapped registers for transparent expansion of a register file	712/32
39	US 59238 71 A	<input type="checkbox"/>	Multifunctional execution unit having independently operable adder and multiplier	712/221
40	US 59192 56 A	<input type="checkbox"/>	Operand cache addressed by the instruction address for reducing latency of read instruction	712/218
41	US 59151 17 A	<input type="checkbox"/>	Computer architecture for the deferral of exceptions on speculative instructions	710/262

UNITED STATES PATENT AND TRADEMARK OFFICE  
CERTIFICATE OF CORRECTION

PATENT NO. : 5,475,853

DATED : December 12, 1995

INVENTOR(S) : Bartholomew Blanner et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:


Col 1 Line 16 Delete "07/579,384" and insert -07/519,384 -

Col 14 Line 62 Delete "bite" and insert -bits-

Col 15 Line 3 Delete "Of" and insert -of-

claim 8

Signed and Sealed this  
Eleventh Day of May, 1999



Q. TODD DICKINSON

Acting Commissioner of Patents and Trademarks

Attesting Officer

Attest:

	Docum ent ID	U	Title	Current OR
42	US 59130 48 A	<input type="checkbox"/>	Dispatching instructions in a processor supporting out-of-order execution	712/215
43	US 59078 60 A	<input type="checkbox"/>	System and method of retiring store data from a write buffer	711/117
44	US 58899 85 A	<input type="checkbox"/>	Array prefetch apparatus and method	712/225
45	US 58871 61 A	<input type="checkbox"/>	Issuing instructions in a processor supporting out-of-order execution	712/244
46	US 58389 40 A	<input type="checkbox"/>	Method and apparatus for rotating active instructions in a parallel data processor	712/216
47	US 58357 47 A	<input type="checkbox"/>	Hierarchical scan logic for out-of-order load/store execution control	712/216
48	US 58092 68 A	<input type="checkbox"/>	Method and system for tracking resource allocation within a processor	712/200
49	US 57991 79 A	<input type="checkbox"/>	Handling of exceptions in speculative instructions	712/234
50	US 57940 29 A	<input type="checkbox"/>	Architectural support for execution control of prologue and epilogue periods of loops in a VLIW processor	712/241
51	US 57548 12 A	<input type="checkbox"/>	Out-of-order load/store execution control	712/216
52	US 57519 85 A	<input type="checkbox"/>	Processor structure and method for tracking instruction status to maintain precise state	712/218
53	US 57198 00 A	<input type="checkbox"/>	Performance throttling to reduce IC power consumption	713/321
54	US 56734 26 A	<input type="checkbox"/>	Processor structure and method for tracking floating-point exceptions	712/244
55	US 56734 08 A	<input type="checkbox"/>	Processor structure and method for renamable trap-stack	712/216
56	US 56597 21 A	<input type="checkbox"/>	Processor structure and method for checkpointing instructions to maintain precise state	712/228
57	US 56551 15 A	<input type="checkbox"/>	Processor structure and method for watchpoint of plural simultaneous unresolved branch evaluation	712/239
58	US 56511 24 A	<input type="checkbox"/>	Processor structure and method for aggressively scheduling long latency instructions including load/store instructions while maintaining precise state	712/215
59	US 56491 36 A	<input type="checkbox"/>	Processor structure and method for maintaining and restoring precise state at any instruction boundary	712/244
60	US 56447 42 A	<input type="checkbox"/>	Processor structure and method for a time-out checkpoint	712/244
61	US 56110 63 A	<input type="checkbox"/>	Method for executing speculative load instructions in high-performance processors	712/205
62	US 55840 09 A	<input type="checkbox"/>	System and method of retiring store data from a write buffer	711/117

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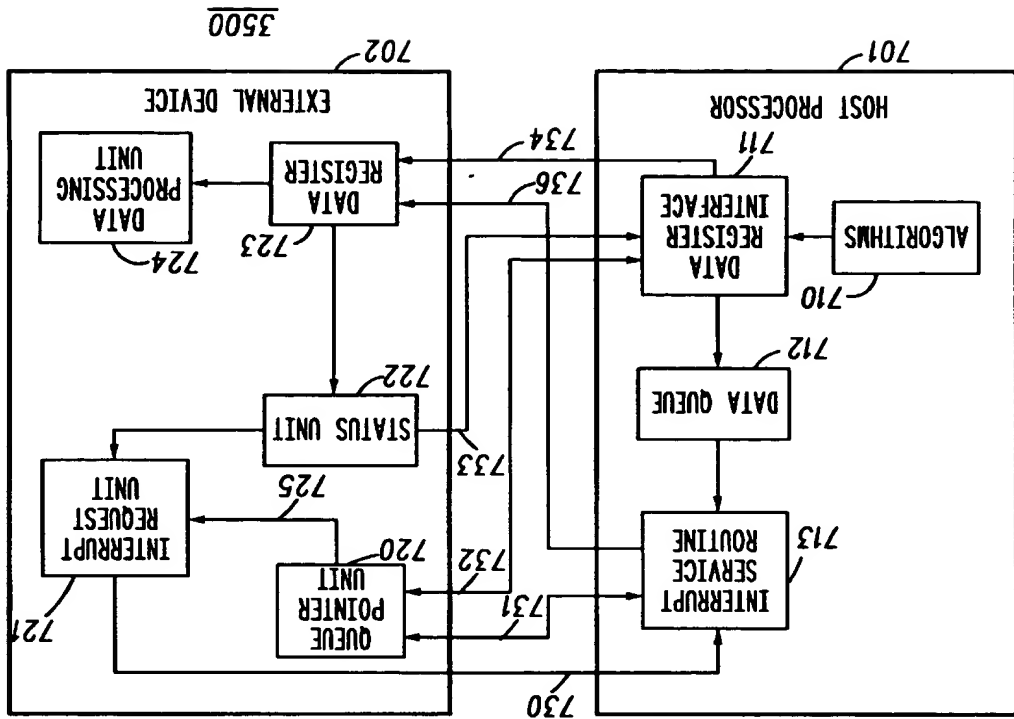
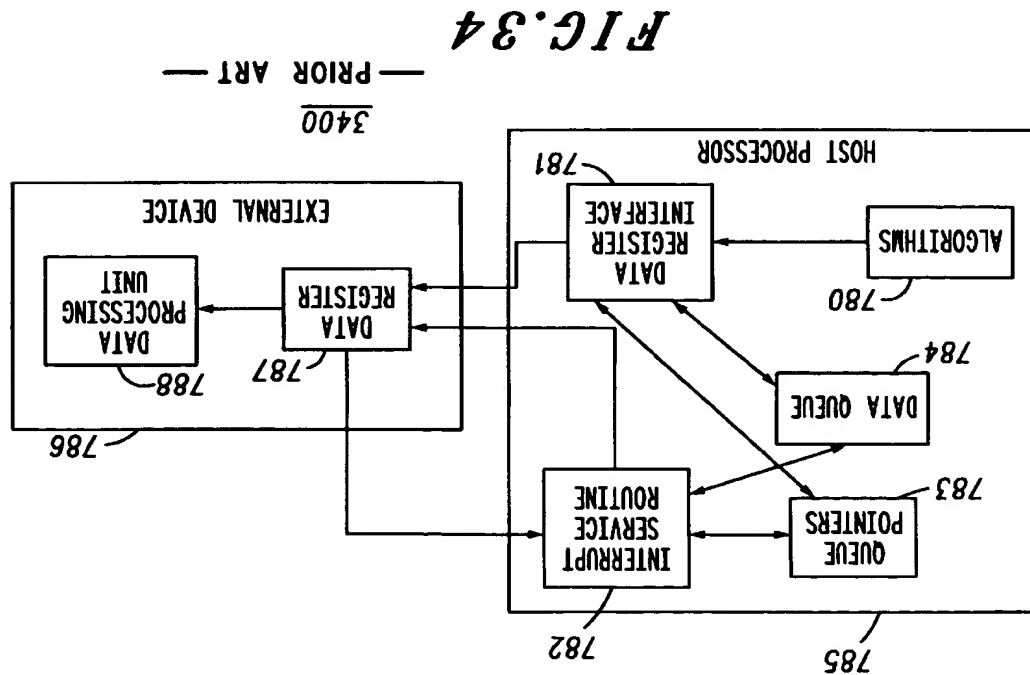
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## Summary

Document	Pages	Printed	Missed	Copies
US005701430	17	17	0	1
US005459844	19	19	0	1
US005475853	17	17	0	1
Total (3)	53	53	0	-



	Docum ent ID	U	Title	Current OR
1	JP 20032 08251 A	<input type="checkbox"/>	ELECTRONIC PROCEDURE EXECUTING PROGRAM AND ELECTRONIC PROCEDURE EXECUTING SERVER	
2	JP 20030 92752 A	<input type="checkbox"/>	MULTIPLEXER, MULTIPLEXING METHOD, IMAGE DECODER AND IMAGE DECODING METHOD	
3	JP 20030 39701 A	<input type="checkbox"/>	PRINTER AND ITS NONPRINT MICROVIBRATION CONTROLLING METHOD	
4	JP 20013 06127 A	<input type="checkbox"/>	JOB INSTRUCTION METHOD	
5	JP 20011 09597 A	<input type="checkbox"/>	NETWORK PRINTING SYSTEM	
6	JP 20001 56868 A	<input type="checkbox"/>	METHOD AND DEVICE FOR DECODING IMAGE	
7	JP 11296 389 A	<input type="checkbox"/>	CONTEXT CONTROLLER FOR MANAGING MULTI-TASKING BY PROCESSOR	
8	JP 11272 383 A	<input type="checkbox"/>	METHOD AND DEVICE FOR GENERATING ACTION SYNCHRONIZED TYPE VOICE LANGUAGE EXPRESSION AND STORAGE MEDIUM STORING ACTION SYNCHRONIZED TYPE VOICE LANGUAGE EXPRESSION GENERATING PROGRAM	
9	JP 11247 689 A	<input type="checkbox"/>	AIR-FUEL RATIO CONTROL DEVICE OF INTERNAL COMBUSTION ENGINE	
10	JP 10266 886 A	<input type="checkbox"/>	FUEL CUT CONTROL DEVICE OF INTERNAL COMBUSTION ENGINE	
11	JP 09223 013 A	<input type="checkbox"/>	SPECULATIVE LOAD INSTRUCTION EXECUTING METHOD FOR HIGH PERFORMANCE PROCESSOR	
12	JP 08298 615 A	<input type="checkbox"/>	ELECTRONIC EQUIPMENT	
13	JP 08171 645 A	<input type="checkbox"/>	METHOD FOR PRODUCING PICTURE AND ITS DEVICE	
14	JP 08171 048 A	<input type="checkbox"/>	CAMERA	
15	JP 08102 365 A	<input type="checkbox"/>	LIGHTING CONTROL SYSTEM	
16	JP 08072 324 A	<input type="checkbox"/>	TAPELIKE LABEL FORMING APPARATUS	
17	JP 08036 407 A	<input type="checkbox"/>	PROGRAMMABLE CONTROLLER AND ITS SFC PROGRAM EXECUTION METHOD	
18	JP 07257 756 A	<input type="checkbox"/>	CONTROL METHOD FOR PICKING OUT POWDERY-GRANULAR MATERIAL	
19	JP 07152 726 A	<input type="checkbox"/>	MODIFIED CHOLESKY DECOMPOSITION CALCULATING DEVICE	
20	JP 06301 099 A	<input type="checkbox"/>	INFORMATION RECORDER FOR CAMERA	



	Docum ent ID	U	Title	Current OR
21	JP 06201 802 A	<input type="checkbox"/>	INTEGRATED CIRCUIT WITH TESTING FUNCTION	
22	JP 06160 042 A	<input type="checkbox"/>	INSTRUCTION METHOD FOR MOUNTED PART INSPECTION DEVICE	
23	JP 06028 198 A	<input type="checkbox"/>	RISC MICROPROCESSOR PRIORITY VECTOR INTERRUPT SYSTEM	
24	JP 05233 276 A	<input type="checkbox"/>	METHOD AND DEVICE FOR SUBMODEL CONTROL IN DATA PROCESSING SYSTEM	
25	JP 05143 858 A	<input type="checkbox"/>	POS TERMINAL	
26	JP 05088 892 A	<input type="checkbox"/>	METHOD AND DEVICE FOR PARALLELLY PROCESSING INFORMATION	
27	JP 05053 836 A	<input type="checkbox"/>	METHOD FOR AUTOMATICALLY DECIDING TASK EXECUTION PRIORITY ORDER	
28	JP 04352 082 A	<input type="checkbox"/>	IMAGE PROCESSOR	
29	JP 04280 263 A	<input type="checkbox"/>	IMAGE FORMING DEVICE	
30	JP 04170 126 A	<input type="checkbox"/>	LINE CONTROL ADAPTOR	
31	JP 03285 569 A	<input type="checkbox"/>	CONTROLLER OF POWER INVERTER	
32	JP 03273 284 A	<input type="checkbox"/>	SCANNING METHOD FOR SCANNING TYPE DISPLAY	
33	JP 03024 560 A	<input type="checkbox"/>	ELECTROPHOTOGRAPHIC DRY TONER	
34	JP 01154 236 A	<input type="checkbox"/>	EXECUTING DEVICE FOR TIME-DIVISION TASK	
35	JP 01135 650 A	<input type="checkbox"/>	DUPLICATE PRINTING INHIBITION METHOD	
36	JP 01133 107 A	<input type="checkbox"/>	SEQUENCE CONTROLLER	
37	JP 01092 843 A	<input type="checkbox"/>	DATA PROCESSING UNIT	
38	JP 01076 486 A	<input type="checkbox"/>	MEMORY IC	
39	JP 01042 751 A	<input type="checkbox"/>	MEMORY CONTROL SYSTEM	
40	JP 63191 346 A	<input type="checkbox"/>	BRAKE MECHANISM	
41	JP 63104 535 A	<input type="checkbox"/>	COMMUNICATION CONTROL METHOD FOR DATA TERMINAL EQUIPMENT	
42	JP 63047 838 A	<input type="checkbox"/>	KNOWLEDGE SUCCESSION CONTROL SYSTEM	
43	JP 62272 314 A	<input type="checkbox"/>	MICROCOMPUTER	

FIG. 37

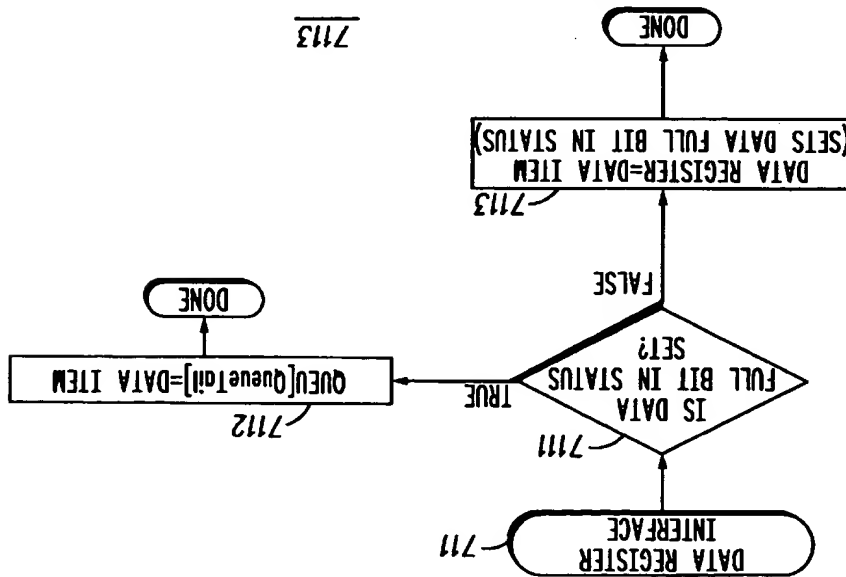
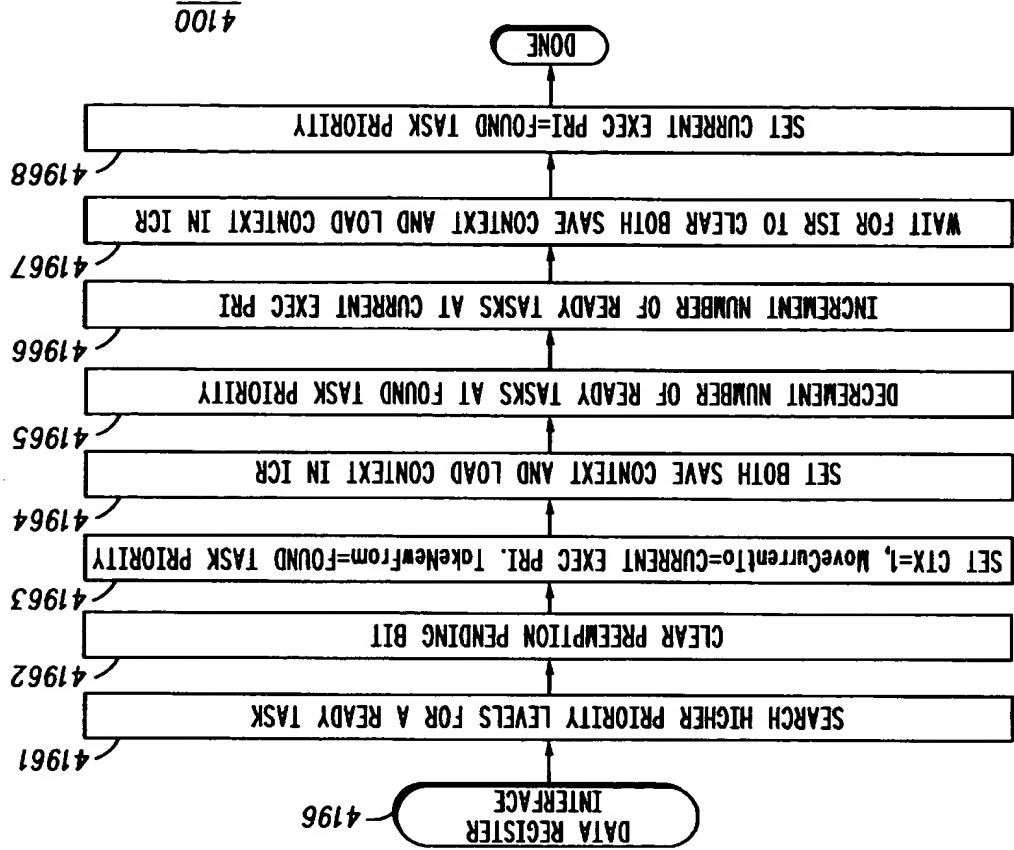
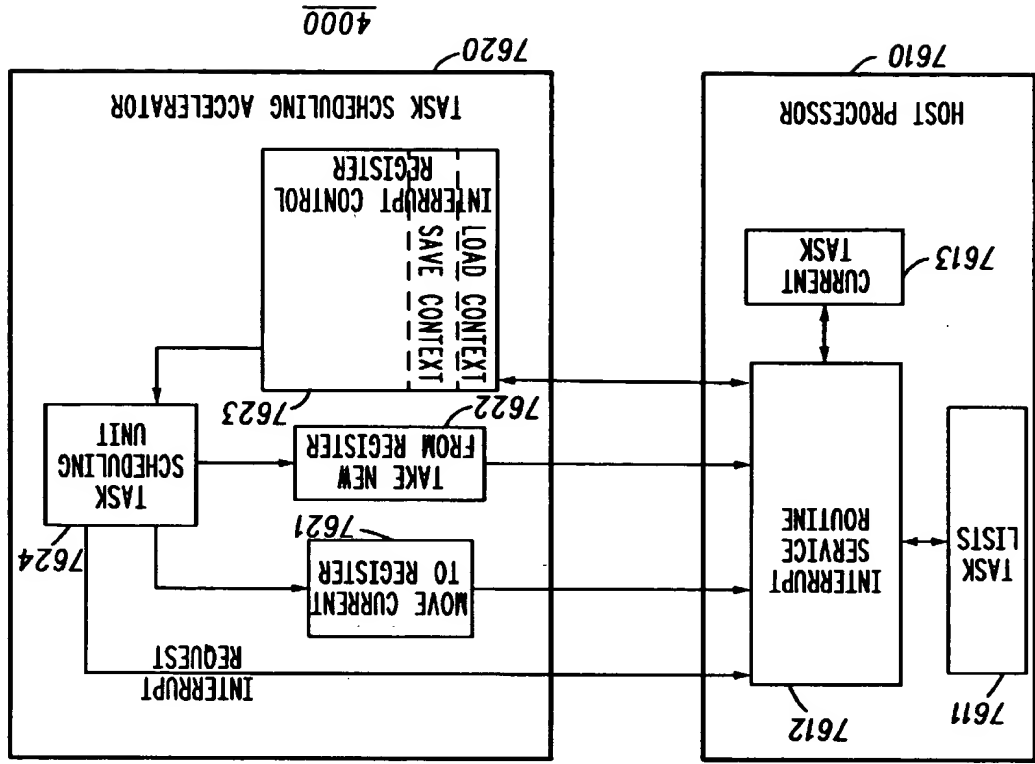
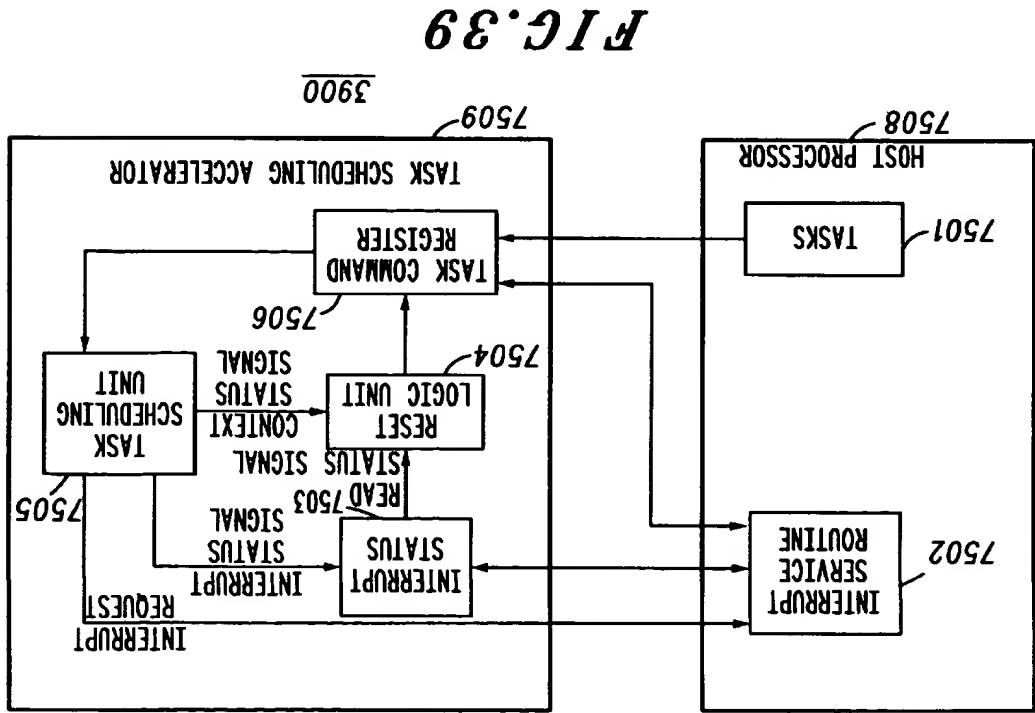


FIG. 41



	Docum ent ID	U	Title	Current OR
44	JP 62197 819 A	<input type="checkbox"/>	DATA TRANSFER CONTROL SYSTEM	
45	JP 62197 818 A	<input type="checkbox"/>	DATA TRANSFER CONTROL SYSTEM	
46	JP 62173 100 A	<input type="checkbox"/>	OPERATING METHOD FOR HYDRAULIC PRESS	
47	JP 62072 045 A	<input type="checkbox"/>	STORAGE PROTECTION KEY CONTROLLER	
48	JP 61099 996 A	<input type="checkbox"/>	DYNAMIC RAM CONTROLLING SYSTEM	
49	JP 60020 211 A	<input type="checkbox"/>	SEQUENCE CONTROLLING DEVICE	
50	JP 59223 463 A	<input type="checkbox"/>	RECORDING DEVICE	
51	JP 59060 645 A	<input type="checkbox"/>	SYSTEM FOR PROCESSING INSTRUCTION EXECUTION OF PROCESSOR	
52	JP 58224 807 A	<input type="checkbox"/>	METHOD FOR CONTROLLING AIR CONDITIONER FOR AUTOMOBILE	
53	JP 58156 250 A	<input type="checkbox"/>	METHOD FOR REPLACING CONTROLLER OF DATA COMMUNICATION NETWORK	
54	JP 58115 552 A	<input type="checkbox"/>	INTERRUPT CONTROLLING SYSTEM	
55	JP 56096 367 A	<input type="checkbox"/>	INFORMATION PROCESSING DEVICE	
56	JP 55043 662 A	<input type="checkbox"/>	ORDER RE-EXECUTION INFORMATION PROCESS SYSTEM	
57	JP 54150 051 A	<input type="checkbox"/>	CHARACTERISTIC TEST DEVICE	
58	JP 54147 388 A	<input type="checkbox"/>	SEQUENCE CONTROLLER	
59	JP 54147 386 A	<input type="checkbox"/>	SEQUENCE CONTROLLER	
60	JP 53121 443 A	<input type="checkbox"/>	INPUT UNIT OF FRONT BUSINESS PROCESSING SYSTEM	
61	EP 13311 39 A2	<input type="checkbox"/>	Information providing apparatus, and method	
62	EP 13108 64 A2	<input type="checkbox"/>	Method and circuit for conditional-flag rewriting control	
63	WO 30072 72 A1	<input type="checkbox"/>	SYSTEMS AND METHODS FOR INTERACTIVE TRAINING OF PROCEDURES	
64	GB 22849 12 A	<input type="checkbox"/>	Data processor with speculative instruction fetching and method of operation	
65	EP 55271 7 A2	<input type="checkbox"/>	Data processing system and method using virtual storage system.	
66	EP 53699 1 A1	<input type="checkbox"/>	Method and apparatus for resynchronizing a moving rotor of a polyphase DC motor.	



	Docum ent ID	U	Title	Current OR
67	EP 43896 1 A2	<input type="checkbox"/>	Hardware data string operation controller.	
68	WO 90147 23 A1	<input type="checkbox"/>	BIT STREAM MACHINE	
69	EP 37600 4 A2	<input type="checkbox"/>	Variable length pipe operations sequencing.	
70	EP 32828 9 A2	<input type="checkbox"/>	IC card and method of writing its operation program.	
71	EP 30170 7 A2	<input type="checkbox"/>	Apparatus and method for providing an extended processing environment on nonmicrocoded data processing system.	
72	EP 25435 2 A1	<input type="checkbox"/>	A programmable machine system.	
73	EP 63458 A2	<input type="checkbox"/>	Microcomputer system.	
74	EP 35647 A2	<input type="checkbox"/>	A SIMD data processing system.	
75	NN961 2119	<input type="checkbox"/>	Instruction Match Function for Processor Performance Monitoring	
76	US 20040 00490 0 A	<input type="checkbox"/>	Dynamic random access memory has local control circuit to generate local control signals based on rise and fall of received main control signals	
77	US 20030 20866 5 A	<input type="checkbox"/>	Cache hit/miss prediction method in pipelined processor, involves reading cache hit/miss prediction value associated with entry corresponding to memory address	
78	WO 20030 91411 A	<input type="checkbox"/>	Obtaining semi-synthetic protein-based site directed probe e.g., ubiquitin vinyl sulfone specific for deubiquitinating enzymes, useful for identification of subset of proteome e.g., ubiquitin/ubiquitin-like proteins	
79	US 20030 18790 5 A	<input type="checkbox"/>	Task sequence scheduling method in word processor, involves maintaining task list containing entry sequence of enabled and disabled tasks and scheduling successive block to be executed after previous block	
80	EP 13315 39 A	<input type="checkbox"/>	Operating method for digital system, by jumping to entry address, executing activation sequence, and entering secure mode.	
81	WO 20030 46715 A	<input type="checkbox"/>	Central processing device e.g. CPU, activates instruction holding unit to set instruction corresponding to selected operating mode in order to acquire firmware	
82	EP 13168 68 A	<input type="checkbox"/>	Electronic control system for an implement towing agricultural vehicle has devices enabling driver during recording mode to record brake signal in addition to recording of sequence of control steps being executed by driver	
83	EP 13108 64 A	<input type="checkbox"/>	Conditional flag rewriting control method for processor e.g. Reduced Instruction Set Computer determines if conditional flag rewriting is enabled or disabled then rewrites/does not rewrite flag as appropriate	
84	WO 20030 32569 A	<input type="checkbox"/>	Server initiated synchronization for third generation CDMA wireless communications that involves server determining maximum size of message to be sent to mobile station for session initiation request	
85	KR 20020 96465 A	<input type="checkbox"/>	Tempo controller of digital audio decoder chip	

DATA TRANSFER USING SOFTWARE  
INTERRUPT SERVICE ROUTINE BETWEEN  
HOST PROCESSOR AND EXTERNAL  
DEVICE WITH QUEUE OF HOST  
PROCESSOR AND HARDWARE QUEUE  
POINTERS ON EXTERNAL DEVICE  
RELATED PATENT APPLICATIONS

The present patent application is related to the following patent applications which are being filed simultaneously (and are hereby incorporated herein) and are assigned to the same entity, Motorola, Inc.: U.S. patent application Ser. No. 09/037,173, still pending, Method, Device and Article of Manufacture for Efficient Task Scheduling in a Multi-tasking Preemptive Priority-Based Real-Time Operating System, by Brett Louis Lindsley; U.S. patent application Ser. No. 09/041,101, still pending, Method, Device and Article of Manufacture for Implementing a Real-Time Task Scheduling Accelerator, by Brett Louis Lindsley, Uri Dayan and Moshe Tarrab; U.S. patent application Ser. No. 09/037,599, still pending, Method, Device and Article of Manufacture for Specifying and Controlling a Task Switch from an External Device in a Multi-Tasking Preemptive Priority-Based Real-Time Operating System, by Brett Louis Lindsley and Ed Martinez; and U.S. patent application Ser. No. 09/041,189, still pending, Method, Device and Article of Manufacture for Clearing Command Bits in a Task Scheduling Device for a Multi-Tasking Preemptive Priority-Based Real-Time Operating System, by Brett Louis Lindsley.

At some time, the currently executing task completes its computation and becomes inactive. A task becomes inactive by pending on a semaphore when the semaphore count is zero or negative. For example, a semaphore may represent data buffers that require processing. If the task that processes data buffers pending for the semaphore that represents data buffers, the task is synchronized to the data buffer generation. If data buffers are available, the semaphore count is greater than zero. Task pend requests on the semaphore allow the task to continue. If data buffers are not available, the semaphore count is less than or equal to zero. When the task pends on the semaphore with a count that is less than or equal to zero, the task does not have data for processing and will block execution.

At the point when a task pends on a semaphore with zero or negative count, the task that has made the request is not allowed to continue execution and must "block". The task scheduling function stops this task and selects another task for execution. The task scheduling function looks at other ready tasks at the same or lower priorities to determine the next highest priority ready task. If a task is found, it is selected for execution. If a task is not found, the processor is put into an idle state until a task becomes ready.

Although the task selection process is easy to understand, in a practical environment this can lead to significant inefficiencies. For example, the following cause inefficiencies in a preemptive prioritized task scheduling system:

Each time a semaphore is processed, there is a potential for a task change. This causes the scheduling function to be called quite often when many times there is no change. When a task pends for a semaphore and blocks, the scheduler must perform a search algorithm to determine the next ready task. If there are a large number of tasks and priority levels, this activity may be time-consuming.

The process of searching for a task may have variable timing making scheduling functions non-deterministic.

A counting semaphore 203 allows a plurality of events to be generated without being lost. Similarly, a plurality of status of the cause of the interrupt.

Events are generated by tasks 201 or interrupt service routines (ISRs) are not allowed to consume events because ISRs are not scheduled and execute outside of the normal task scheduling environment of the processor. However, ISRs are allowed to generate events to indicate the status of the cause of the interrupt.

Scenaphores synchronize the event producer and the event consumer as shown in FIG. 2, numeral 200.

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Scenaphores synchronize the event producer and the event consumer as shown in FIG. 2, numeral 200.



	Document ID	U	Title	Current OR
86	US 20020 15236 8 A	<input type="checkbox"/>	Processor for computer system, executes subsequent instruction according to prediction of value indicating result of execution of instruction	
87	JP 20021 23596 A	<input type="checkbox"/>	Car inspection and registration method using internet, involves performing package management of car owner and mechanic field to enable car inspection agent to execute car inspection and registration process	
88	EP 11687 72 A	<input type="checkbox"/>	Controlling operation of WAP enabled mobile terminal in telecommunication network, incorporating preferential mode selection instruction in sequence of instructions of page of service data	
89	JP 20012 23938 A	<input type="checkbox"/>	Camera with built-in video recording device, has selection unit to choose automatic execution mode to operate device with respect to stored program	
90	US 62302 78 B	<input type="checkbox"/>	Data processing device for audio reproducing system, has processing units with respective instruction sequencers to process sequence of instructions selected from respective memory on receiving instruction directive	
91	US 62124 08 B	<input type="checkbox"/>	Voice controlled interaction enabling for voice mail system, by interpreting audible information from user in voice command mode as voice command instructing communication handset to dial needed key sequence entry	
92	JP 20003 11931 A	<input type="checkbox"/>	Semiconductor integrated circuit for large-scale integration, has test sequencer which activates CPU to execute stored test program of intellectual core property, corresponding to setup mode value in register	
93	GB 23459 80 A	<input type="checkbox"/>	Mode shape converter arranged at terminal of optical device and adapted to couple light via optical fibers, has lower cladding coated over substrate having etched portion with lower rib waveguide over which core is formed	
94	US 60723 95 A	<input type="checkbox"/>	Remote controlled signaling method for use in classrooms, involves activating red, yellow and green lights sequentially, to indicate students about the termination of instruction period	
95	WO 20001 6570 A	<input type="checkbox"/>	Electrostatic radio frequency identification reader/encoder, has exciter that generates and transmits data sequence signal with data sequence received from processor, and clock signal	
96	US 59833 35 A	<input type="checkbox"/>	Multiple out-of-order instructions issuing and execution mechanism in superscalar machine e.g. IBM system	
97	US 59580 45 A	<input type="checkbox"/>	Memory operands specialized fetching method in load store unit for code sequence execution in microprocessor	
98	US 61340 63 A	<input type="checkbox"/>	Multitrack data transfers using disk drive storage device, such as computer disk drive, minimizing microprocessor firmware overhead and reducing amount of track skew	
99	US 58954 92 A	<input type="checkbox"/>	Data integrity protecting method in computer system - involves setting lock field of current lock entry to lock state, if no other lock entry is found to have lock field set in locked state	
100	US 58729 10 A	<input type="checkbox"/>	Parity error injection system for instruction processor in data processing system	
101	JP 10149 295 A	<input type="checkbox"/>	Sequence controller for computer system connected with several copiers - has instruction decoder which decodes from instruction read-out and sets condition execution instruction flag active to read condition execution instruction from memory	
102	US 57404 17 A	<input type="checkbox"/>	Low power pipelined processor - includes BHT storing prediction states receiving branch instruction address and providing entry history bits with pipeline resource switching to low power mode when enable signal received	

The foregoing is a summary and thus contains, by its very nature and by necessity, simplifications, generalizations and omissions of detail. Consequently, the reader will appreciate that the summary is illustrative only and is not intended to be limiting in any way. Other aspects, inventive features, and advantages of the present invention, as defined solely by the claims, will become apparent to one of ordinary skill in the art based on the teachings of the non-limiting detailed description set forth below.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of one embodiment of a device in accordance with the present invention, showing data flow and functionality of the invention.

FIG. 3 shows schematic representations of examples of special function bits in control registers for task commands, interrupt control and status in accordance with the present invention describes.

FIG. 4 is a flow chart showing one embodiment of steps for implementing the operation of the state machine that controls the accelerator in accordance with the present invention.

FIG. 5 is a flow chart showing one embodiment of data flows for executing commands that are synchronous to the task wherein the task must allow the previous command to clear before executing the next command in accordance with the present invention.

FIG. 6 is a flow chart indicating one embodiment of the functions that tasks and interrupts use to control the task scheduling accelerator in accordance with the present inven-

FIG. 7 is a flow chart showing one embodiment of steps for adding a new task to the currently executing task set in the multi-tasking environment in accordance with the present invention.

FIG. 8 is a flow chart illustrating one embodiment of steps for how a task exists to remove itself from the currently-executing task set in the multi-tasking environment in accordance with the present invention.

FIG. 9 is a flow chart showing one embodiment of steps for how a task may modify its own priority in accordance with the present invention.

FIG. 10 is a flow chart showing one embodiment of steps for how a task may yield to another task at the same priority level in accordance with the present invention.

FIG. 11 is a flow chart showing one embodiment of steps for how tasks pend for semaphores on the host processor in accordance with the present invention.

FIG. 12 is a flow chart showing one embodiment of data flows for executing commands that are asynchronous to the task (commands that the task does not need to wait for completion or commands generated by interrupts) in accord-

FIG. 13 is a flow chart showing one embodiment of steps for how seamphores are posted by tasks and interrupts on the dance with the present invention.

manufacturer that optimizes real-time multi-tasking for a processor.

## SUMMARY

A combined hardware and software data queuing mecha-

nism for efficient data transfer from a host processor to an external device is presented. In one embodiment, the host processor maintains a queue of data items and the external device maintains hardware pointers to the queue. Data is

efficiently stored in the host processor's queue by reading the external hardware pointers when the external device data registers are full. Data is efficiently retrieved from the queue and written to the external device by an interrupt service

routine by reading the external hardware pointers. The hardware queue pointers automatically increment and wrap when reaching a maximum value. Placing the queue pointers in hardware releases the software of maintaining the pointers, incrementing them and wrapping them. Since the

external hardware has direct access to the queue pointers, the external hardware device asserts its interrupt to request data from the host processor only when it knows there is data queued in the host processor.

In one embodiment, a device provides efficient transfer of data items between a host processor and an external device. The device includes a host processor and the external device. The host processor is coupled to external queue pointers. The host processor is capable of managing a plurality of pointers. The host processor is capable of managing a plurality of pointers.

The external device is coupled to the host processor for storing and incrementing/decrementing the external device.

In another embodiment, a method for efficient transfer of data items between a host processor and an external device

is provided. The method includes using a host processor which is coupled to external queue pointers for queuing a plurality of data items. The method further includes trans-

terming the plurality of data items to the external device using an interrupt service routine unit, and using the external device which is coupled to the host processor for storing and

In another embodiment, an article of manufacture having

processor and an external device is provided. The device includes the host processor and the external device. The host processor is coupled to external queue pointers for queuing

	Docum ent ID	U	Title	Current OR
103	RD 40818 6 A	<input type="checkbox"/>	Testing method for program activity implementations of work-flow management systems e.g. IBM FlowMark (RTM) - constructing network of activities as coloured graph, with nodes representing activities to be performed and edges potential sequence of their execution, and materialising input container, requesting fields	
104	GB 23100 57 A	<input type="checkbox"/>	Pipeline type information processing apparatus - has instruction read inhibit bit provided for each pair of addresses registered in branch history and instruction read inhibit bit setting section	
105	US 56110 63 A	<input type="checkbox"/>	Selective execution method for CPU speculative load instructions - involves determining bit state in response to load instruction, suspending instruction execution pending branch processor control signals and resetting bit state on execution of instruction	
106	US 56447 42 A	<input type="checkbox"/>	Speculative instruction execution tracking for processor - involves assigning identification tag to each instruction issued with associated activity bit set on issue and cleared on completion	
107	CN 11279 12 A	<input type="checkbox"/>	Speech synthesising device for high level language command decoding	
108	US 55068 21 A	<input type="checkbox"/>	Optical disk program repeater system - has sequence controller sending predetermined set of instructions to disk player in response to power supply, and disk output monitor controlling disc player in response to proprietary code recorded on disk	
109	US 54902 54 A	<input type="checkbox"/>	Integrated circuit for interfacing system with MIL-STD-1533 data bus - uses register-based architecture that allows for autonomous operation in three standard modes simultaneously, with operation of IC being autonomous	
110	US 54835 39 A	<input type="checkbox"/>	High frequency programmable demultiplexer appts. for PCM-TDM data communication - includes FAL hardware controlled by PFAC with decommutation and dejustification function unit with output logic controlled by programmable decommutator sequence	
111	US 54288 02 A	<input type="checkbox"/>	Disc data storage retrieval system controller - has device for executing critical selection start command received from host computer which directs controller flag in on state	
112	US 54169 11 A	<input type="checkbox"/>	Instruction pipeline data processor with load multiple register instruction - stores identity of highest numbered register or registers modified during last execution cycle of multiple register loading instruction with indication of number of registers loaded	
113	EP 61419 3 A	<input type="checkbox"/>	Integrated circuit memory retention fault detection - causing each memory bank to execute three test sequences, each sequence delayed to allow detection or bit pattern from previous sequence	
114	EP 67718 8 B	<input type="checkbox"/>	Instruction tagging for superscaler processor - has tags in FIFO allocated to instructions fetched into execution units and used to monitor program order of instructions and registers used	
115	US 54637 43 A	<input type="checkbox"/>	Actively patching SCSI processor instructions for reselection operation with tagged queues - preparing jump table comprising jump to sequence for each possible tagged queue, obtaining tag value of reselecting queue, preparing jump into jump table having offset from beginning of jump table based on tag value and executing jump	
116	EP 58165 9 A	<input type="checkbox"/>	Computerised navigation system for aircraft - has LAN with central unit controlling access across network and to memory which stores navigation information retrieved and processed by suite of programs while terminals display results	
117	EP 57854 0 A	<input type="checkbox"/>	Function testing of Application Specific Integrated Circuit - using silicon chip with application program connected to central unit with read-only memory to test at time of production	
118	JP 05035 442 A	<input type="checkbox"/>	Data processing appts. with video interface function for serially transferring image data to printer, display - inputs 32-bit image data to thinning out circuit through bus and thins out data to have active data width of 24 bits	

FIG. 14 is a schematic representation of operation of pointer registers for assisting the queuing of semaphore posts in accordance with the present invention.

FIG. 15 is a flow chart showing one embodiment of steps for how the state machine requests semaphore posts to be moved from the queue on the host processor to the task scheduling accelerator in accordance with the present invention.

FIG. 16 is a schematic representation of the data flows and information for the accelerator to signal the host processor and communicate changes in the task execution in accordance with the present invention.

FIG. 17 is a flow chart showing one embodiment of steps for the functions executed by the interrupt service routine on the host processor in accordance with the present invention.

FIG. 18 is a flow chart showing one embodiment of steps for how the interrupt service routine moves a queued semaphore post to the accelerator in accordance with the present invention.

FIG. 19 is a schematic representation of data structures stored on the host processor used to describe the current state of task execution in accordance with the present invention.

FIG. 20 is a schematic representation of how the interrupt interface communicates information that determines how the interrupt service routine switches tasks in accordance with the present invention.

FIG. 21 is a flow chart showing one embodiment of steps for how the interrupt service switches tasks in accordance with the present invention.

FIG. 22 is a schematic representation of how processing on the host processor and task scheduling accelerator overlap to provide efficient task switching in accordance with the present invention.

FIG. 23 is a flow chart showing one embodiment of steps for how the state machine processes adding task requests from the host processor in accordance with the present invention.

FIG. 24 is a flow chart showing one embodiment of steps for how the state machine processes task exit requests from the host processor in accordance with the present invention.

FIG. 25 is a flow chart showing one embodiment of steps for how the state machine processes modify priority requests from the host processor in accordance with the present invention.

FIG. 26 is a flow chart showing one embodiment of steps for how the state machine processes task yield requests from the host processor in accordance with the present invention.

FIG. 27 is a flow chart showing one embodiment of steps for how the state machine processes semaphore pend requests from the host processor in accordance with the present invention.

FIG. 28 is a flow chart showing one embodiment of steps for how the state machine processes semaphore post requests from the host processor in accordance with the present invention.

FIG. 29 is a flow chart showing one embodiment of steps for how the interrupt service routine moves a task between queues in accordance with the present invention.

FIG. 30 is a block diagram illustrating how the task scheduling accelerator is physically connected to a host processor in accordance with the present invention.

FIG. 31 is a block diagram schematic showing one embodiment of how the task scheduling accelerator may be implemented in a hardware configuration in accordance with the present invention.

FIG. 32 is a block diagram schematic showing one embodiment of the state machine that controls the hardware in accordance with the present invention.

FIG. 33 is a schematic representation of examples of encoding of the instructions for the state machine in accordance with the present invention.

FIG. 34 is a block diagram illustrating how data is typically transferred between a software task or interrupt on a host processor to an external device in the prior art.

FIG. 35 is a block diagram illustrating the specific details of implementing an efficient data queuing method.

FIG. 36 is a block diagram illustrating the specific details of how hardware queue pointers operate.

FIG. 37 is a flow chart illustrating the required operations by an interface function on the host processor for either writing data to the external device or queuing the data.

FIG. 38 is a flow chart illustrating how the interrupt service routine efficiently moves data from the host processor to the external device.

FIG. 39 is a block diagram illustrating specific details of how the task command register is cleared.

FIG. 40 is a block diagram illustrating specific details of how the Task Scheduling Accelerator efficiently communicates information about a task switch to the Host Processor.

FIG. 41 is a flow chart illustrating how the Task Scheduling Accelerator selects a task after the task lock has been turned off and higher priority ready tasks are pending.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

The present invention resolves the problems with implementing task scheduling without the need for imposing constraints by moving a selected portion of the task scheduling functionality to an external hardware accelerator. By allowing part of the functionality to remain in software on the host processor, flexibility is maintained without the need of constraints. By moving scheduling decisions to an external accelerator device, fast determination of scheduling decisions is performed. Since the external accelerator device may compute schedule decisions in parallel with activity on the host processor, an overlap of scheduling decisions with host processor activity allows variable or lengthy scheduling decisions to be hidden during host processor activity.

The present invention improves upon prior art hardware devices. Prior art hardware devices store almost all of the information for task scheduling locally in the hardware. To minimize the amount of information stored (and reduce the hardware cost), prior art devices require restrictions to limit the number of tasks, the number of tasks at the same priority level, the range of the semaphore counter, etc.

The present invention improves upon the prior art by providing a method of determining a ready task that is dependent only on the number of priority levels and not the number of tasks. This allows many tasks to be added to the system without an increase in the search time for a ready task. Further, scheduling computations for determining ready tasks is overlapped with the host processor for maximum efficiency. Because scheduling computations are performed externally to the host processor, no entry/exit code is required in interrupt service routines. The present invention

	Docum ent ID	U	Title	Current OR
119	US 51596 76 A	<input type="checkbox"/>	DRAM controller IC providing pseudo-cache mode operation using standard page mode draws - uses logic to enable or disable page mode operation as result of executing software instructions, or prediction of page mode efficiency based on past performance	
120	US 51631 40 A	<input type="checkbox"/>	Branch prediction cache structure responds to input program counter - using two levels that respond to both small and large entry numbers	
121	SU 16653 79 A	<input type="checkbox"/>	Programmed with operative correction execution sequence monitor - includes decoder with outputs connected to corresp. inputs of delay elements	
122	EP 43045 3 A	<input type="checkbox"/>	Error recovery in optical disk cartridge handling system - stopping low level moving function state update flag is set, and recovery is performed after completion of high level moving	
123	EP 42372 6 A	<input type="checkbox"/>	Branch control circuit for pipeline processing of instruction - predicts whether branch is taken and processes instructions addressed by branch before it is taken	
124	EP 41051 6 A	<input type="checkbox"/>	Coding technique for binary data - uses data octets to impose binary encoding to protect data using masking system and correspondence table	
125	EP 40729 5 A	<input type="checkbox"/>	Monitoring of execution of program in computer system - uses access to memory and filtering of I=O transactions to provide selected operational data to external programs	
126	GB 22322 81 A	<input type="checkbox"/>	IC card memory protection and test program - protects predetermined memory region including stored pass code and address restriction circuit on address bus	
127	EP 39793 4 A	<input type="checkbox"/>	Bit stream machine - has orchestrator with program memory, bit controller, LFS sequencer, and multiple bit processor devices	
128	EP 39117 3 A	<input type="checkbox"/>	Debug peripheral for computers microprocessors, and core processor - provides background mode processing capability in existing CPU core without modification to core design	
129	EP 37600 4 A	<input type="checkbox"/>	Sequencing of pipe operations - has two modes so that second can be used when first reaches null stage	
130	EP 35829 3 A	<input type="checkbox"/>	Local area communication transport system - uses broadcasts of services, slot numbers and message sequence numbers to improve transmission of information	
131	EP 34972 6 A	<input type="checkbox"/>	Integrated-circuit card with low power consumption mode - exchanges information with external data processing system, and has microprocessor	
132	EP 31218 3 A	<input type="checkbox"/>	Function capability enhancement in data processing system - provides sixteen-bit and thirty-two bit capabilities to system designed originally for eight-bit capability	
133	EP 30170 7 A	<input type="checkbox"/>	Data processing system using micro-code techniques - has extended processor instruction code mode that disables instructions to interrupt execution of normal instructions	
134	GB 22004 82 A	<input type="checkbox"/>	Monitoring control flow in microprocessor - generating representative interface signal when branch instruction is executed	
135	GB 21924 71 A	<input type="checkbox"/>	Programmable machine system for food mfr. - has computer controlled actuators and compiler program display to enable operator to enter instructions via input	
136	SU 13524 97 A	<input type="checkbox"/>	Data exchange unit - analyses attributes for mode control stored in commands register in control and reception modes	
137	EP 19673 6 A	<input type="checkbox"/>	Microprogram controlled data processing appts. - has made selector to enable operation of faster and slow microprogram sequences of instructions	
138	DE 36104 33 A	<input type="checkbox"/>	Programmed control system for controlling machine - uses stored structural program to fix sequence of contact plan programs	
139	EP 18047 6 A	<input type="checkbox"/>	Single chip micro-programme sequence controller - can be selectively operated in either interrupt or trapped mode	
140	EP 16733 3 A	<input type="checkbox"/>	Digital data processor with data word type classifier - provides respective abbreviated jump field in instruction words to specify branch destinations	

The present invention utilizes a hardware accelerator, herein called a "task scheduling accelerator" (TSA), for improving the performance of real-time task scheduling without imposing constraints on the functionality of the system. An efficient partitioning between the TSA and the host processor software allows functional flexibility while providing acceleration of task scheduling functionality.

The TSA implements a model of task scheduling where tasks are prioritized and lower priority tasks may be preempted if a higher priority task becomes ready. The TSA may execute commands to add a task, exit the current task, yield to another task at the same priority, modify the current task priority, pend for semaphores or post a semaphore. Using these basic functions, real-time operating system functionality may be developed.

The TSA accepts commands from tasks called "synchronous" task commands. These commands are synchronous from the point of view that the task may not issue another synchronous task command until the previous synchronous task command has been completed. It is allowable for the task to perform other activity after issuing a synchronous task command as long as the task verifies the previous synchronous task command has been completed prior to issuing another synchronous task command. The TSA provides the Task Command register to indicate when a synchronous task command has been recognized and clears the status bit when the function is completed.

Interrupts perform functions on the host processor asynchronous to task execution. Since interrupts may generate events by posting semaphores, it is necessary to have a separate mechanism for issuing commands that are asynchronous to tasks. When these "asynchronous" commands are issued, there is no need to wait for them to complete. An important aspect of a system using the TSA is that the TSA may request service from the host processor via an interrupt. This allows the host processor to enter a special mode for processing the interrupt request. At this time, the currently executing task has been preempted and a new task can be selected simply by changing to a new context. A task switch is performed by saving the context of the current task and loading the context of a new task. The context is defined as all the registers used by the task and any shared resources. Thus, a task switch involves saving all processor registers and shared resources used by the currently executing task and loading a new set of processor registers and shared resources for the new task.

A task command may cause the current task to be preempted. An example of when this occurs is when a task pends for a semaphore, but the semaphore count is zero or negative. The TSA preempts the currently executing task with an interrupt and switches to another task. Eventually, the task that was preempted becomes ready to execute. When the task continues executing, it determines the TSA status bit is clear and continues. The task is completely unaware preemption has taken place and other tasks were not minimized exposure of the task scheduling functionality to the application program.

	Docum ent ID	U	Title	Current OR
141	EP 16724 1 A	<input type="checkbox"/>	Microprogram sequence controller with comparator register - has comparator which stores instruction address for comparison with generated instruction address on output data bus	
142	EP 15053 5 A	<input type="checkbox"/>	Loop instruction data processor - uses counter, address register, program counter, clock, ROM, instruction register and loop counter	
143	US 45218 50 A	<input type="checkbox"/>	Instruction buffer associated with cache memory unit - stores data group sequence for current procedure while simultaneously storing instruction sequence identified by transfer command	
144	AU 84323 01 A	<input type="checkbox"/>	Multi-mode scanning appts. for host and secondary computers - executes sequence of modes by having address of ram scanned into register, and has data transfer between locations permitted using interface	
145	EP 13248 1 A	<input type="checkbox"/>	Elastic buffer memory for digital multiplex data transmission - indicates RAM address sequence for active channels and extracts micro-instructions at clock rate greater than arrival rate	
146	EP 11177 6 A	<input type="checkbox"/>	Interrupt controller for instruction pipelined digital processor - has instruction clarification system with interrupt class decoder for each machine instruction and has interrupt sequence detector	
147	EP 12677 4 A	<input type="checkbox"/>	Microcomputer control system for two-bed desiccant dryer - receives moisture indication from capacitance probes and adjusts regeneration cycle accordingly	
148	DE 32414 12 A	<input type="checkbox"/>	Testing advanced direct memory access controller - by using CPU or externally accessing integral test register through sequencer	
149	US 44400 59 A	<input type="checkbox"/>	Sound responsive lighting device with VCO driven indexing - sequentially activates each of LEDs, connected to indexer, in which execution speed is proportional to intensity of sound field	
150	US 44307 06 A	<input type="checkbox"/>	Branch prediction for data processor - monitors instruction flow and provides record in prediction memory which is accessed using hash coded version	
151	EP 98970 A	<input type="checkbox"/>	Numerical controller for grinding machine - controls machining of cylindrical portions formed on rotating workpiece and has two feed devices responsive to pulse generator	
152	EP 59952 A	<input type="checkbox"/>	Motor vehicle mounted controller - has vocal enunciator to enable occupant to select radio-stereo unit and air conditioning options	
153	US 43420 82 A	<input type="checkbox"/>	Program instruction mechanism for shortened recursive handling - sets condition code distinguishing between pending and non-pending request for interruption	
154	EP 35647 A	<input type="checkbox"/>	SIMD parallel array data processor - performs for registration of processing and machine status and activity masks to control execution status	
155	FR 24481 23 A	<input type="checkbox"/>	Microprocessor controls rotation sequence of pistol targets - using sequences stored in replaceable memory which may easily be changed	
156	SU 76580 9 B	<input type="checkbox"/>	Self-diagnosing microprogram processor - has decoder at output of AND-gate with inputs from error-identifying flip=flop and micro-command counter	
157	DE 29112 98 B	<input type="checkbox"/>	PCM digital transmission system fault location - using long block words of zeros and loop back line testing through regenerators	



2 that is typically implemented in hardware. The TSA contains registers for control/status or to specify a particular integer value. The control/status registers are shown in FIG. 3, numeral 300.

The Task Command register 301 indicates synchronous task commands issued by tasks on the host processor. These bits include:

Add Task—This bit is set to add a task to the current task set.

Task Exit—This bit is set to exit the currently executing task.

Modify Priority—This bit is set when the currently executing task changes its priority.

Task Yield—This bit is set to yield to another task at the same priority level.

Semaphore Pend—This bit is set when a task makes a pend request.

Task Lock—This bit specifies a mode of operation where the TSA will not preempt the current task. This is typically used to protect critical regions of programs that share data between multiple tasks. When the bit is cleared, the TSA is allowed to preempt the task.

These bits are described in further detail when covering the functions that use them.

The Interrupt Control register 302 specifies the reason for the TSA interrupt to the host processor. There are three major functions this register controls:

Move Post—This is an indication the TSA-ISR is to move a semaphore post index from the semaphore index queue to the asynchronous task command interface.

There is no change in the currently executing task.

Move Task—This is an indication to move a task from one task list to another. There is no change in the currently executing task.

Load Context—Indicates if the context of a new task should be loaded.

Idle—Indicates the task set is idle.

These bits are described in further detail when covering the functions that use them.

The Status register 303 specifies additional status information to the host processor or the TSA. These bits include:

CTX—This bit indicates if the TSA-ISR should treat the Task Command register as context (preserve it) or not as context (modify it). This bit is used to clear command bits in the Task Command register during a context switch.

Semaphore Post—This bit indicates a task or interrupt service routine has written a semaphore post to the asynchronous task command interface.

IDLE—This bit is used to retain the state of the task set being in the idle (no active tasks) state.

Preemption Pending—This bit is set to indicate the current task will be preempted when it turns off the task lock. This bit is set by the TSA if a semaphore is posted with a higher priority ready task pending when the task lock is enabled.

These bits are described in further detail when covering the functions that use them.

When the system is reset, the TSA begins execution of its internal State Machine 41 as indicated in FIG. 4, numeral 400. At initialization 411, the State Machine 41 enters a loop checking for a function to execute with comparisons 4120, 4130, 4140, 4150, 4160, 4170. The loop checking includes: Is Sem Pend set in the TCR (Task Command Register)? 4120; Is Sem Post set in Status? 4130; Is Add Task set in TCR? 4140; Is Task Exit set in TCR 4150; Is Task Yield set in TCR? 4160; Is Modify Priority set in TCR? 4170. Does S/W queue have sem posts and are post registers empty? 4170; and, Is the task lock off and the preemption pending bit set? 4195. If any comparison is true, the TSA processes the true function 4122, 4132, 4142, 4152, 4162, 4172, 4196 and returns to the beginning of the loop to check Is Sem Pend set in the TCR 4120. If all comparisons are false, the TSA does not have any functions to process and enters a low power mode 4180 until there is activity. Each of the functions of the State Machine 41 are explained in further detail later. Activity that brings the State Machine 41 out of low power 4180 is any of the loop conditions being true. Since the state machine is turned off when in low power, activity is detected by direct hard-wired logic to the state machine. This is shown in detail in FIG. 32 where signals Sema160000, Sema160001, Sema160002, Sema160003, Sema160004, Sema160005, Sema160006, Sema160007, Sema160008, Sema160009, Sema160010, Sema160011, Sema160012, Sema160013, Sema160014, Sema160015, Sema160016, Sema160017, Sema160018, Sema160019, Sema160020, Sema160021, Sema160022, Sema160023, Sema160024, Sema160025, Sema160026, Sema160027, Sema160028, Sema160029, Sema160030, Sema160031, Sema160032, Sema160033, Sema160034, Sema160035, Sema160036, Sema160037, Sema160038, Sema160039, Sema160040, Sema160041, Sema160042, Sema160043, Sema160044, Sema160045, Sema160046, Sema160047, Sema160048, Sema160049, Sema160050, Sema160051, Sema160052, Sema160053, Sema160054, Sema160055, Sema160056, Sema160057, Sema160058, Sema160059, Sema160060, Sema160061, Sema160062, Sema160063, Sema160064, Sema160065, Sema160066, Sema160067, Sema160068, Sema160069, Sema160070, Sema160071, Sema160072, Sema160073, Sema160074, Sema160075, Sema160076, Sema160077, Sema160078, Sema160079, Sema160080, Sema160081, Sema160082, Sema160083, Sema160084, Sema160085, Sema160086, Sema160087, Sema160088, Sema160089, Sema160090, Sema160091, Sema160092, Sema160093, Sema160094, Sema160095, Sema160096, Sema160097, Sema160098, Sema160099, Sema160100, Sema160101, Sema160102, Sema160103, Sema160104, Sema160105, Sema160106, Sema160107, Sema160108, Sema160109, Sema160110, Sema160111, Sema160112, Sema160113, Sema160114, Sema160115, Sema160116, Sema160117, Sema160118, Sema160119, Sema160120, Sema160121, Sema160122, Sema160123, Sema160124, Sema160125, Sema160126, Sema160127, Sema160128, Sema160129, Sema160130, Sema160131, Sema160132, Sema160133, Sema160134, Sema160135, Sema160136, Sema160137, Sema160138, Sema160139, Sema160140, Sema160141, Sema160142, Sema160143, Sema160144, Sema160145, Sema160146, Sema160147, Sema160148, Sema160149, Sema160150, Sema160151, Sema160152, Sema160153, Sema160154, Sema160155, Sema160156, Sema160157, Sema160158, Sema160159, Sema160160, Sema160161, Sema160162, Sema160163, Sema160164, Sema160165, Sema160166, Sema160167, Sema160168, Sema160169, Sema160170, Sema160171, Sema160172, Sema160173, Sema160174, Sema160175, Sema160176, Sema160177, Sema160178, Sema160179, Sema160180, Sema160181, Sema160182, Sema160183, Sema160184, Sema160185, Sema160186, Sema160187, Sema160188, Sema160189, Sema160190, Sema160191, Sema160192, Sema160193, Sema160194, Sema160195, Sema160196, Sema160197, Sema160198, Sema160199, Sema160200, Sema160201, Sema160202, Sema160203, Sema160204, Sema160205, Sema160206, Sema160207, Sema160208, Sema160209, Sema160210, Sema160211, Sema160212, Sema160213, Sema160214, Sema160215, Sema160216, Sema160217, Sema160218, Sema160219, Sema160220, Sema160221, Sema160222, Sema160223, Sema160224, Sema160225, Sema160226, Sema160227, Sema160228, Sema160229, Sema160230, Sema160231, Sema160232, Sema160233, Sema160234, Sema160235, Sema160236, Sema160237, Sema160238, Sema160239, Sema160240, Sema160241, Sema160242, Sema160243, Sema160244, Sema160245, Sema160246, Sema160247, Sema160248, Sema160249, Sema160250, Sema160251, Sema160252, Sema160253, Sema160254, Sema160255, Sema160256, Sema160257, Sema160258, Sema160259, Sema160260, Sema160261, Sema160262, Sema160263, Sema160264, Sema160265, Sema160266, Sema160267, Sema160268, Sema160269, Sema160270, Sema160271, Sema160272, Sema160273, Sema160274, Sema160275, Sema160276, Sema160277, Sema160278, Sema160279, Sema160280, Sema160281, Sema160282, Sema160283, Sema160284, Sema160285, Sema160286, Sema160287, Sema160288, Sema160289, Sema160290, Sema160291, Sema160292, Sema160293, Sema160294, Sema160295, Sema160296, Sema160297, Sema160298, Sema160299, Sema160300, Sema160301, Sema160302, Sema160303, Sema160304, Sema160305, Sema160306, Sema160307, Sema160308, Sema160309, Sema160310, Sema160311, Sema160312, Sema160313, Sema160314, Sema160315, Sema160316, Sema160317, Sema160318, Sema160319, Sema160320, Sema160321, Sema160322, Sema160323, Sema160324, Sema160325, Sema160326, Sema160327, Sema160328, Sema160329, Sema160330, Sema160331, Sema160332, Sema160333, Sema160334, Sema160335, Sema160336, Sema160337, Sema160338, Sema16